Code No: G6809/R13

M.Tech. I Semester Supplementary Examinations, January-2017

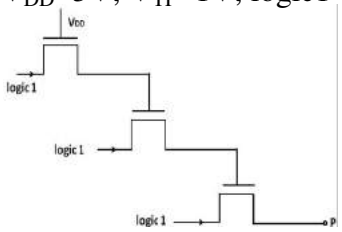
CMOS DIGITAL IC DESIGN

(Common to VLSI & ES, ES & VLSI, VLSID & ES, ES & VLSID, VLSI, VLSID, VLSISD and VLSI&ME)

Time: 3 hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1.	a	Explain and derive the necessary DC region equations of a CMOS inverter.	6M
	b	Explain the DC noise margin of CMOS logic.	6M
2.	a	Write short notes on transmission gates with the relevant circuits.	6M
	b	Bring out the differences between Pass Transistor logic and transmission gate logic.	6M
3.	a	Design and explain the operation of 2 input NMOS NAND.	6M
	b	Explain the procedure to design an adder circuit using CMOS logic.	6M
4.		Explain voltage boots trapping with an example.	12M
5.	a	Explain the concept of charge storage and charge leakage associated with pass transistor logic.	6M
	b	Find the value at the point P mentioned in the circuit shown in above figure for the given values V_{DD}=5V; V_{TP}=1V; logic1=5V and explain it.	6M



6.	a	Draw the D latch by using CMOS logic and explain its operation in detail.	6M
	b	Write short notes on SR latch in sequential MOS logic.	6M
7.	a	Write notes on pseudo NMOS logic gate.	6M
	b	Write notes on Ferro electric Random Access Memory (FRAM).	6M
8.	a	Write about the leakage currents in SRAM.	6M
	b	Explain NOR flash memory.	6M

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