Subject Code: H3802/R13

M. Tech –II Semester Regular Examinations, September, 2014

ADVANCED COMPUTER ARCHITECTURE

(Common to DECS, E&CE and DECE)

Time: 3 Hours **Max Marks: 60**

Answer any FIVE questions

All questions carry EQUAL marks

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1. a) Explain the Changing faces of computing and task of computer designer.
   b) What is the memory addressing methodology of computer design from relevant instruction set? Explain in detail.

2. a) Briefly Explain how operations are performed in the instruction set.
   b) Explain Amdahl's law and elaborate how the speedup is quickly calculated using Amdahl's law.

3. a) Elaborate the classic five stage pipelined RISC processor with a neat diagram.
   b) Explain the Dynamic scheduling in detail.

4. a) How we reduce the cache miss penalty in Memory hierarchy design.
   b) Explain the Dynamic scheduling using Tomasulo's approach.

5. a) Draw and explain the flow of memory hierarchy design, in detail.
   b) Illustrate Instruction Level Parallelism VLIW software approach with suitable example.

6. a) Briefly Explain Systematic shared memory architecture.
   b) Explain the characteristics of DECS, ECE and DECE51.

7. a) Draw and explain the operation of Intel based IA-64 Instruction Level Parallelism processor.
   b) What are the practical issues raised in interconnecting networks?

8. a) Write short notes on Designing of clusters.
   b) Write short notes on distributed shared memory.

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