Code No: **RT41041** **R13** **Set No. 1**

IV B.Tech I Semester Regular Examinations, November - 2016

VLSI DESIGN

(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B

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PART–A ***(22 Marks)***

1. a) What are the steps involved in IC fabrication. [4]
   b) Draw the circuit diagram for CMOS two-input NAND gates. [4]
   c) Define Fan-in and Fan-out. [3]
   d) Write about pass transistor and pass transistor gates. [4]
   e) Write note on package solution. [4]
   f) What is the need of a FPGA? And write its applications. [3]

PART–B ***(3x16 = 48 Marks)***

2. a) Explain about various IC technologies [8]
   b) Explain the term output conductance, using necessary equations. [8]

3. a) Design a stick diagram for NMOS EX-OR gate. [8]
   b) Draw the mask layout of 1-bit CMOS shift register cell. [8]

4. a) Define inverter delay? Explain. [8]
   b) Define scaling factor? Explain different types of device parameters. [8]

5. a) Explain the design of a 4-bit shifter. [8]
   b) Discuss the general arrangement of a 4-bit arithmetic process. [8]

6. a) Explain mixed signal design with neat sketch. [8]
   b) Discuss the clock mechanisms [8]

7. a) Explain the basic architecture of FPGA. [8]
   b) Explain the FPGA design process. [8]

Code No: **RT41041** **R13** **Set No. 2**

IV B.Tech I Semester Regular Examinations, November - 2016

VLSI DESIGN

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Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B

*****

PART–A ***(22 Marks)***

1. a) Explain the figure of merit of a MOS transistor. [4]
   b) What are scalable design rules and list its disadvantages. [4]
   c) What are the sources of wiring capacitances? [3]
   d) Explain charge storage. [4]
   e) What is testing? Explain. [4]
   f) Write the steps to design an FPGA. [3]

PART–B ***(3x16 = 48 Marks)***

2. a) Explain the MOS transistor operation with the help of neat sketches in the Enhancement mode. [8]
   b) Explain how the BiCMOS inverter performance can be improved. [8]

3. a) What are the different types of design rules? Explain. [8]
   b) What is a stick diagram? Draw the stick diagram and layout for a CMOS inverter. [8]

4. a) Explain briefly about sheet resistance? [8]
   b) Discuss the limits due to subthreshould current. [8]

5. Explain bus arbitration logic for n-line bus structured design approach. [16]

6. a) Explain the single Stuck-at Fault model. [8]
   b) Discuss the ASIC design flow. [8]

7. a) How to design FPGA-Based PCBs? Explain. [8]
   b) Write about FPGA families of different vendors. [8]

Code No: **RT41041** **R13** **Set No. 3**

IV B.Tech I Semester Regular Examinations, November - 2016

VLSI DESIGN

(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B

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PART–A ***(22 Marks)***

1.	a)	Draw the basic circuit of NMOS and CMOS inverter.	[4]
	b)	What are absolute design rules?	[4]
	c)	List out the limitations of scaling?	[3]
	d)	What is pre-charged bus concept?	[4]
	e)	Give the advantages and disadvantages of cell based design.	[4]
	f)	Write about configuration modes.	[3]

PART–B ***(3x16 = 48 Marks)***

2.	a)	Derive the expression for the threshold voltage of MOSFET.	[8]
	b)	Explain the MOS transistor operation with the help of neat sketches in the Depletion mode.	[8]
3.		Draw the stick diagram and mask layout for CMOS two input NOR gate and stick diagram of two input NAND gates.	[16]
4.	a)	Discuss about nMOS transistor as a switch and pMOS transistor as a switch.	[8]
	b)	Define standard unit capacitance? Explain.	[8]
5.	a)	Explain two-phase clocking.	[8]
	b)	Discuss some system considerations.	[8]
6.	a)	Give the overflow of system on chip designs.	[8]
	b)	Explain the FPGA design flow.	[8]
7.		Explain stack implementation using VHDL.	[16]

Code No: **RT41041** **R13** **Set No. 4**

IV B.Tech I Semester Regular Examinations, November - 2016

VLSI DESIGN

(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B

Answer ALL sub questions from Part-A

Answer any THREE questions from Part-B

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PART–A (22 Marks)

1. a) Compare CMOS with bipolar technologies. [4]
   b) Draw the circuit diagram for CMOS two-input NOR gates. [4]
   c) What are the advantages and disadvantages of dynamic logic? [3]
   d) Write about dynamic register element. [4]
   e) Write the steps to resolve the clock skew problem. [4]
   f) What parameters to be consider while identifying the FPGA? [3]

PART–B (3x16 = 48 Marks)

2. a) Explain different steps involved in the IC fabrication? [8]
   b) Draw the circuit for nMOS inverter and explain its operation and characteristics [8]

3. a) Explain MOS layers with a neat sketch. [8]
   b) Explain 2µm CMOS design rule for wires? [8]

4. a) What are the limits on logic levels and supply voltage due to noise in scaling? [8]
   b) Realize the NAND gate using nMOS technology. [8]

5. a) Explain the structured design approach of parity generator. [8]
   b) Explain switch logic? [8]

6. a) Discuss the design process for developing a chip. [8]
   b) Compare Full-Custom design with semi-custom design. [8]

7. Explain implementation of queue using VHDL. [16]