Code No: **RT41044** **R13** **Set No. 1**

IV B.Tech I Semester Supplementary Examinations, March - 2017

COMPUTER ARCHITECTURE & ORGANIZATION

(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B

Answer ALL sub questions from Part-A

Answer any THREE questions from Part-B

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PART–A *(22 Marks)*

1. a) Convert the number $(7654)_8$ to hexadecimal. [3]
   b) Write about Reduced Instruction Set Computer. [4]
   c) Define micro program. [3]
   d) Write about virtual memory. [4]
   e) Define source -initiated transfer using handshaking. [4]
   f) Define cache coherence. [4]

PART–B *(3x16 = 48 Marks)*

2. a) Briefly write about **r's** complement and **(r-1)'s** complement. [8]
   b) Explain any two ways of adding decimal numbers. [8]

3. a) Discuss about stack organization of memory. Give its applications. [8]
   b) Briefly write about instruction codes. [8]

4. a) A computer has **16** registers, an ALU with **32** operations and a shifter with eight operations, all connected to a common bus
      i) Formulate a control word for a micro operation
      ii) Specify the number of bits in each field of control word and give a general encoding scheme [10]
   b) Differentiate hard wired control unit and micro programmed control unit. [6]

5. a) Explain Set Associative mapping for organizing cache memory. [8]
   b) Consider the following reference string: **1 2 3 4 1 2 5 1 2 3 4 5**, apply FIFO page replacement algorithm and calculate number of page faults by considering **3** frames. [8]

6. a) Differentiate Isolated I/O and memory mapped I/O. [8]
   b) Explain daisy chain priority interrupt. [8]

7. a) Write in detail about inter processor communication and synchronization. [8]
   b) Explain the concept of pipelining for floating - point addition and subtraction. [8]