Code No: **RT41044** **R13** **Set No. 1**

IV B.Tech I Semester Regular Examinations, November - 2016

COMPUTER ARCHITECTURE & ORGANIZATION

(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
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PART–A *(22 Marks)*

1.	a)	Write the structure of buses used in computer system?	[3]
	b)	List out the typical logical and bit manipulation instructions.	[4]
	c)	Write about the fetch routine in symbolic microinstructions.	[3]
	d)	Differentiate logical and physical address representations.	[4]
	e)	Write about first-in and first-out buffers in asynchronous data transfer.	[4]
	f)	What is inter- process arbitration?	[4]

PART–B *(3x16 = 48 Marks)*

2.	a)	Explain various number systems and number representations used in system.	[8]
	b)	Dividend A=01110 Divisor B=10001. Explain flowchart for divide operation.	[8]
3.	a)	What is the purpose of addressing modes? Explain various addressing mode techniques.	[8]
	b)	Design and explain 4-bit adder-subtractor and 4-bit arithmetic circuit to perform addition and subtraction using full adders.	[8]
4.	a)	Explain micro sequencer organization with a neat sketch.	[8]
	b)	Discuss the following: Computer configuration for micro program, Symbolic micro program and binary micro program.	[8]
5.	a)	Explain Cache memory organization with Associative mapping? Explain how it improves the memory access time?	[8]
	b)	What is the need for replacement? Explain various cache block replacement algorithms.	[8]
6.	a)	Show internal configuration of a DMA controller diagrammatically and explain how it's working.	[8]
	b)	Explain about Prioritized Interrupts and interrupts cycle.	[8]
7.	a)	Write about i) No-operations ii) instruction reordering iii) annulling	[8]
	b)	What is cache coherence problem? Explain various protocols to handle it.	[8]

Code No: **RT41044** **R13** **Set No. 2**

IV B.Tech I Semester Regular Examinations, November - 2016

COMPUTER ARCHITECTURE & ORGANIZATION

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Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
*****

PART–A *(22 Marks)*

1. a) How to estimate the performance of software? [3]
   b) What is high impedance state in bus buffer? [4]
   c) Explain the format of micro instruction. [3]
   d) What is segmented page mapping? [4]
   e) Write about parallel priority interrupts. [4]
   f) List out the typical characteristic of multiprocessors. [4]

PART–B *(3x16 = 48 Marks)*

2. a) Perform the subtraction of Unsigned numbers using 10's and 2's compliment. Give at least two examples. [8]
   b) Explain the process of multiplying binary integers with Booth's algorithm. [8]

3. a) Define micro-operation and explain the four Basic types of shift micro-operation and their variants. [8]
   b) Consider the arithmetic statement X= (A+B)*(C+D). Explain the influence of number of addresses on computer program. [8]

4. a) Explain the organizations of micro programmed control unit with neat sketch. [8]
   b) What is address sequencing? Explain the conditional branching and mapping of instruction in it. [8]

5. a) Explain Cache with Set-Associative and direct mapping. Assume your own example address and explain. [8]
   b) Explain how memory management unit provides memory protection. [8]

6. a) Explain Types of Interrupts with an example for each. [8]
   b) Explain with a neat diagram, system configuration incorporating an I/O processor. [8]
7. a) Explain how to resolve branch conflicts in Instruction pipeline. [8]
   b) Discuss various inter connection structures available for multiprocessor systems. [8]

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Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
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PART–A (22 Marks)

1. a) What is fixed point representation? [4]
   b) How to specify the internal organization of a digital computer? [3]
   c) Write short notes on conditional branching. [4]
   d) Define pages, blocks and page frames. [4]
   e) What is data transparency? [3]
   f) Define delayed load and delayed branch. [4]

PART–B (3x16 = 48 Marks)

2. a) Convert the $(256)_{10}$ into following codes
      i) Binary Coded Decimal (BCD) ii) Excess 3 codes
      iii) Gray code iv) Reflected Code [8]
   b) Explain addition and subtraction algorithms for data represented in signed-magnitude and signed 2's compliment. [8]

3. a) Explain the following with respect to stack organization
      i) Register stack ii) Stack Operations iii) Reverse Polish Notation [9]
   b) With neat sketch explain the design of control unit of basic computer. [7]

4. a) Write the format of the micro instruction and micro operations for the control memory. [8]
   b) Explain the mapping from instruction code to micro instruction address. Give the first micro instruction for the 0010, 1011 and 1111. [8]

5. a) Explain how the logical address is translated into physical address in paging. [10]
   b) Explain the relationship between address and memory space in virtual memory system. [6]

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6. a) Explain the following with respect to serial communication: Character oriented protocol and Bit Oriented protocol. [8]
   b) What are the handshaking signals? Explain handshake control of data transfer during input and output operations. [8]

7. Write short notes on the following
   a) Parallel Arbitration [5]
   b) Matrix multiplication using vector processing. [5]
   c) RS232 serial Interface. [6]

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Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B

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PART–A *(22 Marks)*

1. a) Write about alphanumeric codes. [3]
   b) What is register-reference instruction? [4]
   c) What is the role of control memory in micro programmed control? [4]
   d) What is content addressable memory? [3]
   e) Differentiate isolated I/O and Memory mapped I/O. [4]
   f) Write short notes on three segment instruction pipeline. [4]

PART–B *(3x16 = 48 Marks)*

2. a) How to represent the signed integer numbers? Perform arithmetic addition and subtraction using 2's compliment. In this how to handle overflow? [8]
   b) Multiplicand B=10111, Multiplier A= 10011. Explain the hardware implementation and algorithm for multiply operation. [8]

3. a) Explain the complete design of simple system to implement RTL code using direct connections, bus and tri-state buffers. [8]
   b) What are the different phases a basic computer instruction cycle consists? Explain instruction cycle with flowchart. [8]

4. a) Explain the design of control unit. How to decode the micro operation fields? Explain the process. [8]
   b) Write the differences between hardwired control and micro programmed control? Is it possible to have a hardwired control associated with a control memory? [8]

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5. a) Explain Cache with associative and two way Set- Associative mapping with a line size of 4 bytes. [10]
   b) What are the techniques used to write Data into the Cache? [6]

6. a) Explain different types of I/O communication techniques with merits and demerits. [8]
   b) What is the need for I/O Processor? Explain the working style of I/O processor. [8]

7. a) Explain different physical forms available to establish inter-connection between various functional units in multiprocessor systems. [8]
   b) With neat sketch explain Time Shared Common Bus Organization and also discuss its merits and demerits. [8]