## B.Tech II Year I Semester (R13) Supplementary Examinations June 2015 ELECTRONIC DEVICES AND CIRCUITS

(Common to EEE, ECE \& EIE)
Time: 3 hours
Max. Marks: 70
PART - A
(Compulsory Question)
1 Answer the following: ( $10 \times 02=20$ Marks)
(a) Define transformer utilization factor.
(b) Define mass action law.
(c) Define amplification factor.
(d) What is pitch-off voltage?
(e) What is DC load line?
(f) Write the relation between S and $\mathrm{S}^{\prime}$.
(g) Draw the h -parameter equivalent circuit for transistor.
(h) Define input impedance.
(i) State any two applications of LCD's.
(j) State the disadvantages of LED.

PART - B
(Answer all five units, $\mathbf{5 \times 1 0} \mathbf{= 5 0}$ Marks)
UNIT - I
(a) Sketch and explain a family of CB output characteristics for a transistor.
(b) Indicate the active, cut-off and saturation regions. Explain the shapes of the curves qualitatively.

## UNIT - III

6 (a) Derive the expression for $\mathrm{I}_{\mathrm{C}}$ versus $\mathrm{I}_{\mathrm{B}}$ for a CE transistor configuration in the active region.
(b) For $\mathrm{I}_{\mathrm{B}}=0$, what is $\mathrm{I}_{\mathrm{C}}$.

OR
In the voltage divider bias circuit, if $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE}}=5 \mathrm{~V}, \mathrm{I}_{\mathrm{C}}=1.2 \mathrm{~mA}, \mathrm{R}_{2}=10 \mathrm{~K}, \beta=100$ In the voltage divider bias circuit, if $\mathrm{V}_{C C}=10 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE}}=5 \mathrm{~V}, \mathrm{I}_{\mathrm{C}}$
and $R_{E}=270 \Omega$ calculate $R_{1}$ and $R_{3}$. Assume $\mathrm{V}_{\mathrm{BE}}$ (active) $=0.6 \mathrm{v}$.
(a) Derive the expression for $A_{V}$ in terms of $A_{1}$.
(b) In terms of the h parameters and the source resistance, derive the equation for the output

OR
Find $h_{r e}$ in terms of the CB $h$ parameters.
UNIT - V


OR
Draw and explain the energy band diagrams for extrinsic semiconductor.
OR
Explain the working of bridge rectifier. Give the expressions for RMS current, PIV, ripple factor and efficiency.

## UNIT - II

Explain with the help of neat diagram the structure of an N -channel FET. In what ways it is different from a bipolar transistor.

OR

> UNIT - IV

## admittance.

