Code: 13A04303

R13/SS

B.Tech II Year II Semester (R13) Supplementary Examinations December/January 2015/2016

SWITCHING THEORY & LOGIC DESIGN

(Common to EEE and ECE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) State and Prove consensus theorem.

(b) Find the 2's complement of representation of -9.

(c) Design a XOR gate using minimum number of NAND gates.

(d) Find the minimum number of literals for the following function using 2 variable Karnaugh Map.
F = =∑m (1) + d (3). d - Don't care.

(e) Write the sum and carry expression for half adder.

(f) Implement the function F =∑m (0, 2) using a 2 × 4 decoder.

(g) Write the characteristic equation for JK Flip-flop.

(h) How many states are there in a n-bit ring counter?

(i) Compare PROM & PAL.

(j) What is meant by cycle in asynchronous circuits?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Express the following function F = xy + x' y in a product of max-terms.

(b) Check if NOR gate is associative or not.

OR

3 (a) Show that a positive logic NAND gate is a negative logic OR gate

(b) Obtain the truth table of the following function and express in sum of min-terms and product of max-terms: F = (A' + B).(B' + C).

UNIT – II

4 Simplify the Boolean function using K map technique:

(a) F = π M (3, 4, 6, 7, 11, 12, 13, 14, 15).

(b) F = ∑m (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14).

OR

5 Simplify the following Boolean function using tabulation method:
F = ∑m (0, 1, 2, 3, 5, 7, 8, 10, 14, 15).

UNIT – III

6 Design a 4-Bit Magnitude comparator using logic gates.

OR

7 (a) Implement the function F = ∑m (0, 1, 2, 4, 5, 8, 11, 12, 15) using 8:1 multiplexer.

(b) Design a half subtractor using logic gates.

UNIT – IV

8 Design a 4 bit universal shift register with neat diagram.

OR

9 Design a 3 bit synchronous up counter using T Flip-flops.

UNIT – V

10 Implement the following functions using PLA with three inputs, four product terms and two outputs.
F1 (A, B, C) = ∑m (3, 5, 6, 7), F2 (A, B, C) = ∑m (0, 2, 4, 7).

OR

11 Implement the switching function F = ∑m (1, 3, 5, 7, 8, 9, 14, 15) by a static hazard free two level AND-OR network.

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