

B.Tech II Year II Semester (R13) Supplementary Examinations May/June 2017

**SWITCHING THEORY & LOGIC DESIGN**

(Common to EEE and ECE)

Time: 3 hours

Max. Marks: 70

**PART - A**

(Compulsory Question)

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- 1 Answer the following: (10 X 02 = 20 Marks)
- Convert the decimal number 250.5 to base 3, base 4.
  - Write and prove de-Morgan laws.
  - Implement two input EX-OR gate from 2 to 1 multiplexer.
  - What are don't cares?
  - Write the block diagram of 3-8 decoder.
  - Implement two input EX-OR gate from 2 to 1 multiplexer.
  - What are the applications of flip flops?
  - How do you build a latch using universal gates?
  - Discuss about a bidirectional shift register.
  - List the advantages of having equivalent states.

**PART - B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT - I**

- 2 (a) Deduce  $(70.65)_8 = ( )_2 = ( )_{16}$   
 (b) Explain 1's complement representation of signed number.

**OR**

- 3 (a) Deduce X from the following:  
 (i)  $(BA0.C)_{16} = (X)_8$ . (ii)  $(7562)_8 = (X)_2$ . (iii)  $(FFE.C)_{16} = (X)_2$ .  
 (b) Convert  $(0011001.0101)_2$  to decimal and octal.

**UNIT - II**

- 4 Implement the following function with NAND gates  $F(x, y, z) = \Sigma(0, 6)$ .

**OR**

- 5 Simplify the following using Tabular method.  
 $F(A, B, C, D, E) = \Sigma(0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 2, 31)$

**UNIT - III**

- 6 Draw the logic diagram for 4 bit binary adder-subtractor circuit and explain its operation.

**OR**

- 7 Implement  $F(A, B, C, D) = \Sigma(0, 1, 3, 5, 6, 8, 9, 11, 12, 13)$  using 8: 1 MUX and explain its procedure.

**UNIT - IV**

- 8 Draw the circuit diagram of MOD-10 counter and explain the operation of it.

**OR**

- 9 With the aid of external logic, convert D type flip flop to a JK flip flop.

**UNIT - V**

- 10 (a) Write the programming table to implement BCD to Z using a PLA.  
 (b) Describe briefly how PAL is used to implement logic functions.

**OR**

- 11 Design and implement full adder with PLA.

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