Code: 13A04303 **R13/SS**

B.Tech II Year II Semester (R13) Supplementary Examinations December 2016

SWITCHING THEORY & LOGIC DESIGN

(Common to EEE and ECE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Perform $(24)_{10} - (56)_{10}$ using 10's complement method.

(b) Represent given function $f = AB + A\overline{C} + \overline{B}C$ into standard SOP form.

(c) Minimize the function F=∑m(2,4,6) using K-map.

(d) Realize the function $F = XY + \overline{X} \cdot \overline{Y} + \overline{Y} \cdot Z$ with NAND and inverter gates.

(e) Implement the function F=∑m (1, 2, 3, 7) using 3:8 decoder.

(f) Implement full subtractor using de-multiplexer.

(g) Draw the logic diagram for 3-stage asynchronous counter with negative edge triggered flip-flops.

(h) Define race around condition in JK flip flop and how it can be eliminated.

(i) Give the logic implementation of a 32*4 bit ROM using decoder of a suitable size.

(j) Define essential hazards in asynchronous circuits.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Complete the following conversions between the number systems:

(i) $(42)_5 = (\ )_7$ (ii) $(1001100110)_2 = (\ )_8$ (iii) $(7E2C)_{16} = (\ )_2$ (iv) $(38.65)_{10} = (\ )_2$

OR

3 Reduce the Boolean expression:

(i) $F = \overline{\left(\overline{X} \cdot \overline{Y} + Z\right)} + Z + XY + WZ$ into three literals.

(ii) $F = \overline{A} \cdot \overline{C} + ABC + A \cdot \overline{C} + A \cdot \overline{B}$ into two literals.

UNIT – II

4 Simplifying the given expression using tabulation method:

F(W,X,Y,Z)=∑m(1,2,3,5,9,12,14,15)+∑d(4,8,11).

OR

5 Minimize the following expressions using K-map and realize using logic gates:

(i) F=∑m(0,7,8,9,10,12)+d(2,5,13)

(ii) F=∑M(0,2,3,8,9,12,13,15).

UNIT – III

6 Implement the following Boolean function with 8:1 multiplexer:

F(A,B,C,D)=∑m(0,2,6,10,11,12,13)+∑d(3,8,14).

OR

7 Design a 8-bit BCD adder using 4-bit binary adder.

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UNIT – IV

8 Design divide by 6 counter using T-flip-flops. Write state table and reduce the expression using k-map.

OR

9 Draw the circuit of JK & SR flip-flops using NAND gates and explain its operation with the help of its characteristic table.

UNIT – V

10 Tabulate the PLA programming table for the four Boolean function listed below:
$F_1(A,B,C,D)=\sum m(3,5,6,7)$, $F_2(A,B,C,D)= \sum m(0,2,4,7)$.

OR

11 For given machine find the corresponding reduced machine table in standard form.

PS	NS,Z	
	X=0	X=1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

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