**Code: 13A04306** **R13**

B.Tech II Year I Semester (R13) Supplementary Examinations June 2016

**DIGITAL LOGIC DESIGN**

(Common to CSE & IT)

Time: 3 hours Max. Marks: 70

**PART – A**

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Draw the truth table of the function F = xy + xy' + y'z

(b) What is the advantage of 2's complement representation of data?

(c) What are universal logic gates, realize AND, OR gates using universal gates?

(d) Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction: (i) X –Y. (ii) Y - X using 2's complements.

(e) Give comparisons between combinational and sequential logic circuits.

(f) Construct the full adder circuit using two half adders.

(g) Write the difference between latches and flip-flops.

(h) Write the difference between synchronous and asynchronous counters.

(i) Write a short note on programmable array logic.

(j) Give the comparison between PROM and PLA.

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

2 (a) Convert (9 B 2 .1A) Hexadecimal to its decimal equivalent

(b) Convert (4310)5 to decimal

(c) Convert $(4021.2)_5$ to its equivalent decimal

(d) Convert 0.640625 decimal numbers to its octal equivalent

**OR**

3 Reduce the following Boolean Expressions to the indicated number of literals:

(a) A'C'+ABC+AC'+AB' to two literals.

(b) (X'Y'+Z')+Z+XY+WZ to three literals.

(c) A'B(D'+CD)+B(A+A'CD) to one literal.

**UNIT – II**

4 Simplify the following Boolean function, using five variable maps:

F(A,B,C,D,E)=∑(0,1,4,5,16,17,21,25,29)

**OR**

5 Simplify the following Boolean function F, together with don't-care conditions d, and then express the simplified function in sum-of-minterms form:

F(A,B,C,D)= ∑(0,6,8,13,14) d(A,B,C,D)= ∑(2,4,10)

**UNIT – III**

6 Design a combinational circuit with three inputs and one output:

(a) The output is 1 when the binary value of the inputs is less than or equal to 3.the output is 0 otherwise.

(b) The output is 1 when the binary value of the inputs is an even number.

(c) The output is 1 when the binary value of the inputs is an odd number.

**OR**

7 (a) Design a 4-bit adder-subtractor circuit and explain the operation in detail.

(b) Explain the functionality of a multiplexer.

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**UNIT – IV**

8 Explain the working of the following:
(a) J-K flip-flop.
(b) S-R flip-flop.
(c) D-flip-flop.

**OR**

9 Explain the design of a 4-bit binary counter with parallel load in detail.

**UNIT – V**

10 (a) Given the 8-bit data word 01011011, generate the 13-bit composite word for the hamming code that corrects single errors and detects double errors.
(b) Write about error detection and correction.

**OR**

11 Write about the following:
(a) Transistor-transistor logic (TTL)
(b) Emitter-coupled Logic (ECL)
(c) CMOS logic

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