Code: 13A04306 **R13**

B.Tech II Year I Semester (R13) Supplementary Examinations November/December 2016

DIGITAL LOGIC DESIGN

(Common to CSE & IT)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Convert the following numbers to decimal: (i) $(1010.011)_2$. (ii) $(630.4)_8$.

(b) Simplify the following Boolean function to a minimum number of literals: $xy + x'z + yz$.

(c) Simplify the Boolean function: $F = x'yz + x'yz' + xy'z' + xy'z$

(d) Write graphic symbols for NAND gate.

(e) Implement OR gate using NAND gate.

(f) Implement OR gate using multiplexer.

(g) Show characteristic equation of JK-FF.

(h) What are the applications of shift register?

(i) Define PAL and PLA.

(j) Compare TTL and CMOS logic.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) With a neat block diagram, explain digital computer.

(b) Express the Boolean function $F = xy + x'z$ in a product of maxterms form.

OR

3 (a) Explain switching circuit that demonstrates binary logic.

(b) Discuss digital logic families.

UNIT – II

4 (a) Simplify the Boolean function using k-map:

(i) $\mathrm{F(w,x,y,z)} = \Sigma(0,1,2,4,5,6,8,9,12,13,14)$.

(ii) $\mathrm{F = A'B'C' + B'CD' + A'BCD' + AB'C'}$

(b) Implement following function using NAND gates: $\mathrm{F(x,y,z)} = \Sigma(0,6)$.

OR

5 Implement the following function using NOR gates: $\mathrm{F(x,y,z)} = \Sigma(0,6)$.

UNIT – III

6 (a) Realize the function $\Sigma\mathrm{m}(0,3,5,6,7)$ using 8:1 multiplexer.

(b) With neat diagram, explain decimal adder.

OR

7 (a) With neat diagram, explain 3 to 8 line decoder.

(b) Implement a full-adder circuit with a decoder and two OR gates.

UNIT – IV

8 (a) With a neat diagram, explain master slave JK Flip Flop.

(b) Explain clocked RS flip-flop.

OR

9 Design a 3-bit MOD-5 synchronous counter using JK-FFs.

UNIT – V

10 (a) A combinational circuit is defined by the functions:

$F_1(A,B,C) = \Sigma(3,5,6,7)$

$F_2(A,B,C) = \Sigma(0,2,4,7)$

Implement the circuit with a PLA having 3 inputs, four product term and two inputs.

(b) Explain CMOS as inverter.

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OR

11 (a) With a neat diagram, explain TTL.

(b) Explain logic construction of a 32 X 4 ROM.

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