Code: 13A04508

R13

B.Tech III Year I Semester (R13) Supplementary Examinations June 2016

LINEAR & DIGITAL IC APPLICATIONS

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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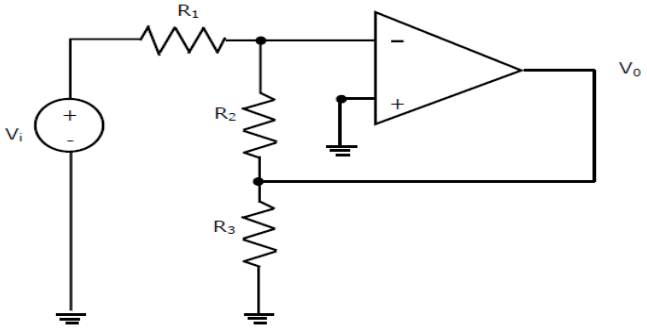
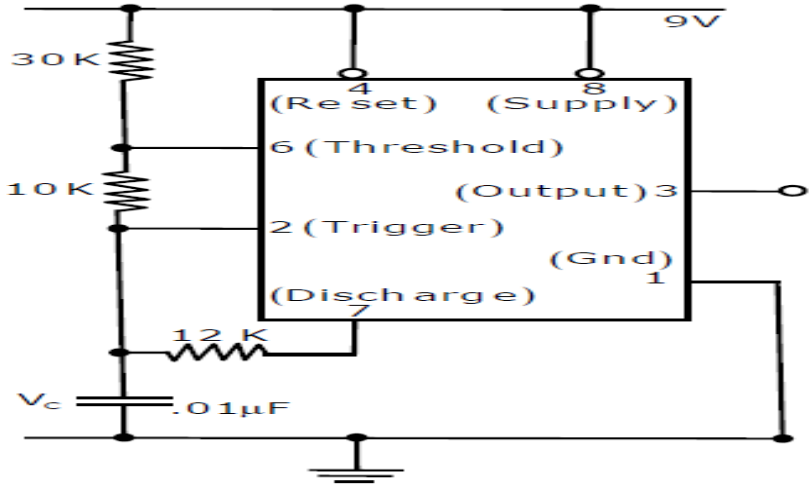
1 Answer the following: (10 X 02 = 20 Marks)

(a) Assuming the OP-AMP to be ideal, the voltage gain of the amplifier shown below is



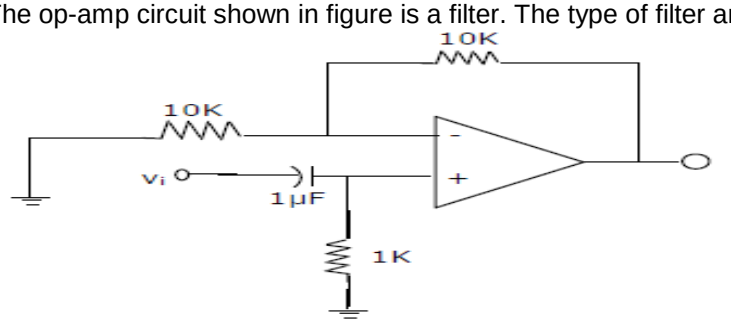
(b) How does negative feedback compensate for a decrease in open loop gain?

(c) An astable multi vibrator circuit using IC 555 timer is shown below. Assume that the circuit is oscillating steadily, find the voltage V_C across the capacitor varies between.



(d) Calculate the values of the LSB, MSB and Full scale output for an 8-bit DAC for the 0 to 10 V.

(e) The op-amp circuit shown in figure is a filter. The type of filter and it's cutoff frequency respectively .



(f) What is an all pass filter? Where and why it is needed?

(g) When do we prefer open collector TTL gate?

(h) Which is fastest logic gate and why?

(i) Why asynchronous inputs are required in flip-flops?

(j) Write about serial binary adder.

Contd. in page 2

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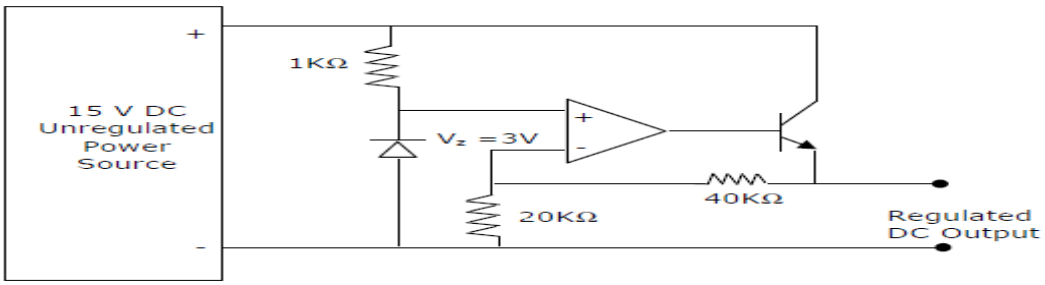
PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

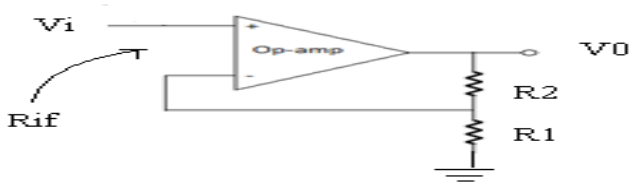
2 (a) Derive an expression for the output voltage and gain of a non-inverting op-amp.

(b) The output voltage of the regulated power supply shown in figure is:



OR

3 (a) Show that input impedance of a non-inverting op-amp of figure below is: $R_{if} = R_i \left(1 + \frac{R_1}{(R_1+R_2)} A_v\right)$. Where R_i is input resistance of an op-amp and A_v is open loop gain and output resistance $R_0 = 0$.

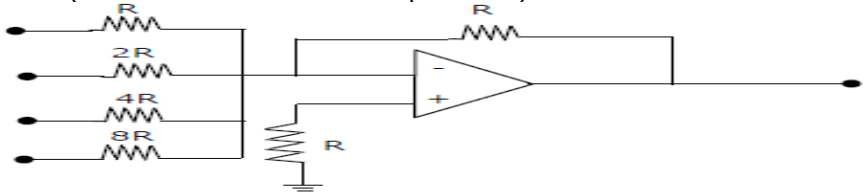


(b) What is the purpose of sample and hold circuit? Explain the working principle of sample and hold circuit using an op-amp.

UNIT – II

4 (a) Configure a 555 timer as a Schmitt trigger and explain. Mention some of its applications.

(b) The circuit shown is a 4-bit DAC the input bits 0 and 1 are represented by 0 V and 5 V respectively. The op-amp is ideal and all the resistances and the 5 V input have a tolerance of + or –10%. The specification(rounded to the nearest multiple of 5%) for the tolerance of the DAC is:



OR

5 (a) Explain frequency translation and FSK demodulation using 565 PLL.

(b) An 8-bit ADC is capable of accepting an input unipolar (positive values only) voltage 0 to 10 V. Find what the minimum value of 1LSB is & what is the digital output code if the applied input voltage is 5.4V?

UNIT – III

6 (a) Derive an expression for the transfer function of a second order low pass Butterworth filter.

(b) Explain VCO? Mention applications of it.

OR

7 (a) Explain the terms: (i) Roll of factor. (ii) Damping coefficient.

(b) Explain, how to obtain triangular wave using a square wave generator?

UNIT – IV

8 (a) Differentiate different logic families and mention their advantages and disadvantages.

(b) Describe TTL driving CMOS and CMOS driving TTL, interfacing techniques.

OR

9 (a) Draw the circuit of Totem-pole TTL NAND gate. What is the purpose of using a diode at the output?

(b) Design a TTL three state NAND gate and explain the operation.

UNIT – V

10 (a) What is a decoder? Explain 3 to 8 line decoder with its truth table.

(b) Design a 3-bit binary synchronous counter.

OR

11 (a) What is parity generator? Explain the 3-bit even parity generator.

(b) Explain different types of shift registers.

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