Code: 13A04508 **R13**

B.Tech III Year I Semester (R13) Regular & Supplementary Examinations November/December 2016

LINEAR & DIGITAL IC APPLICATIONS

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) What is an OPAMP?

(b) What is the need of an instrumentation amplifier?

(c) What is meant by PLL? Write any two applications of PLL.

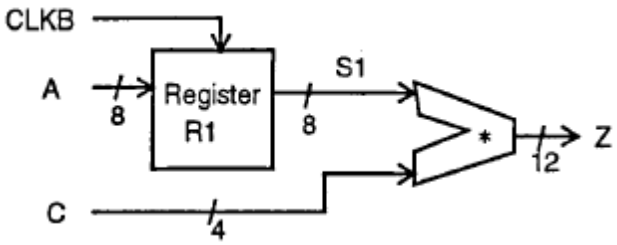
(d) What are the applications of an OP-AMP comparator?

(e) List out important characteristics of digital IC's.

(f) Classify the bipolar logic family by operation and give examples for each category.

(g) What are the various steps in an HDL-based design flow?

(h) Consider the circuit shown in Figure below, that saves the value of the input A into a register and then multiplies it with input C. Write the entity declaration that declares the interface signals for the circuit.



(i) What is a shift register?

(j) What is a PLD? Write the classification of PLDs?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) List out ideal OP-AMP characteristics.

(b) Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to 1 kHz.

OR

3 (a) What are the main features of IC 741 OP-AMP?

(b) Design an inverting amplifier with an input resistance of 10 kΩ and gain of -5.

UNIT – II

4 (a) Design an astable multivibrator using an OP-AMP to generate a frequency of 1 kHz.

(b) Draw the diode based log amplifier diagram and its output characteristics.

OR

5 (a) What is a Schmitt trigger? Draw the circuit of Schmitt trigger using 555 timer and explain its operation briefly.

(b) What are the two basic modes in which the 555 timer operates? Briefly explain the differences between the two operating modes of 555 timer.

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UNIT – III

6 (a) Draw the CMOS 2-input AND gate circuit diagram and function table.

(b) Explain CMOS dynamic electrical behaviour in terms of transition time, propagation delay and power dissipation.

OR

7 (a) Explain the principle of a Emitter-Coupled Logic (ECL/CML) through Basic ECL inverter/buffer circuit with input HIGH and LOW.

(b) What are the advantages and disadvantages of ECL?

UNIT – IV

8 (a) Draw the VHDL programs file structure and explain the same with the syntax of a VHDL entity declaration and architecture definition.

(b) Explain structural, data flow and behavioral modelling styles using VHDL with suitable examples.

OR

9 (a) Write the syntax of a VHDL component declaration and by making use of component declaration, write a VHDL program for a prime-number detector.

(b) Write the syntax of a VHDL process statement and by making use of process statements, write a process-based dataflow VHDL architecture for the prime-number detector.

UNIT – V

10 Draw the logic symbol, truth table, logic diagram of a commercially available MSI 74 x 138 3-to-8 binary decoder and model the same using data flow-style VHDL program.

OR

11 Draw the traditional logic symbol, truth table, logic diagram of a standard MSI 74 x 194 4-bit, Universal Shift Register and model the same using data flow-style VHDL program.

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