

B.Tech IV Year I Semester (R13) Supplementary Examinations June 2017

VLSI DESIGN

(Common to ECE & EIE)

Time: 3 hours

Max. Marks: 70

PART – A

(Compulsory Question)

1 Answer the following: (10 X 02 = 20 Marks)

- (a) What is Moore's law? State various IC technologies on the basis of number of transistors on a chip.
- (b) Define threshold voltage with suitable equation of a MOS device.
- (c) What is the figure of merit of a MOS transistor? Mention the suitable expression for figure of merit.
- (d) Design a stick diagram for NMOS inverter.
- (e) Explain working of pass transistor logic.
- (f) Design a two input CMOS NAND gate with neat sketch.
- (g) Explain the working of a magnitude comparator.
- (h) Compare CPLD and FPGA.
- (i) Write a short note on design capture tools.
- (j) Explain controllability and observability.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Explain NMOS fabrication process flow with neat diagrams.

OR

3 Draw V-I characteristics of NMOS transistor. Explain its operation. Derive the drain to source current equation in saturation and resistive region.

UNIT – II

4 Design a stick and layout diagram for CMOS inverter and two input n-MOS NAND

OR

- (a) Define fan-in and fan-out. Explain their effects on propagation delay.
- (b) What do you mean by inverter delay? Explain.

UNIT – III

6 What are the alternate gate circuits are available, explain them with suitable sketch?

OR

7 Explain about VLSI physical design floor planning.

UNIT – IV

8 Implement arithmetic logic unit to perform both arithmetic and logic functions using a full adder.

OR

9 Explain the design flow of FPGA.

UNIT – V

- (a) What is meant by synthesis? Explain the circuit synthesis design methods.
- (b) What is meant by Simulation? Explain the various VHDL simulations.

OR

11 Explain various design capture and verification tools.
