Code: 13A04701 **R13**

B.Tech IV Year I Semester (R13) Supplementary Examinations June 2018

VLSI DESIGN

(Common to ECE & EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) What is Moore's law? State various IC technologies on the basis of number of transistors on a chip.

(b) Describe the different operating regions for an MOS transistor.

(c) What is figure of merit of a MOS transistor? Mention suitable expressions for figure of merit.

(d) What are the limitations of scaling?

(e) Explain working of pass transistor logic.

(f) What are the different ways to improve clock distribution?

(g) Explain working of magnitude comparator.

(h) What are the advantages and applications of FPGA?

(i) What are the different types of modeling in VHDL?

(j) Explain controllability and observability.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Explain clearly about NMOS fabrication process flow with neat diagrams.

OR

3 Draw the V-I characteristics of MOSFET and prove that I_{ds} is linear function of V_{ds}.
When the gate to source voltage V_{GS} of a MOSFET with threshold voltage of 400 mv, working in saturation is 900 mv, the drain current is observed to be 1 mA and assuming that the MOSFET is operating at saturation, calculate the drain current for an applied V_{GS} of 1400 mv.

UNIT – II

4 (a) Define fan-in and fan-out. Explain their effects on propagation delay.

(b) What do you mean by inverter delay? Explain.

OR

5 Design a stick and layout diagram for CMOS inverter and two inputs NMOS NAND gate.

UNIT – III

6 What are the alternate gate circuits are available? Explain them with suitable sketch.

OR

7 Discuss about the floor planning.

UNIT – IV

8 Explain the working principle of 6-transistor static RAM and 1-transistor dynamic RAM with necessary diagrams.

OR

9 Explain in detail about design flow of FPGA.

UNIT – V

10 Explain the design capture and design verification tools.

OR

11 What is meant by synthesis? Explain the circuit synthesis design methods.

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