Code: 15A04301 **R15**

B.Tech II Year I Semester (R15) Regular Examinations November/December 2016

ELECTRONIC DEVICES & CIRCUITS

(Common to EEE, ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Briefly write about diode resistance.
(b) Write major differences between zener breakdown and avalanche breakdown.
(c) Define TUF & PIV.
(d) Define & Classify filters.
(e) Briefly explain reach through effect.
(f) Draw the symbols for NPN (BJT), PNP (BJT), N-channel JFET and P-channel JFET.
(g) What is the importance of biasing?
(h) Write short notes on thermal runaway.
(i) Sketch the transistor hybrid model.
(j) Draw small signal model for FET.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Derive diode current equation.
(b) A silicon diode has a saturation current of 7.5 μA at room temperature 300 K. Calculate the saturation current at 400 K.

OR

3 Explain construction and operation of UJT & SCR with necessary diagrams.

UNIT – II

4 Explain construction and operation of a bridge rectifier and derive its expressions.

OR

5 (a) Discuss full wave rectifier with L-section filter.
(b) Design a filter for full wave rectifier circuit with LC filter to provide an output voltage of 10 V with a load of 200 mA and the ripple is limited to 2%.

UNIT – III

6 Draw and explain characteristics of Common Collector configurations.

OR

7 Explain construction and operation of N-channel Enhancement & Depletion mode MOSFET.

UNIT – IV

8 Why self bias technique is so popular? And derive its three stability factors.

OR

9 What is the difference between bias stabilization & bias compensation? And also explain any two methods of bias compensation.

UNIT – V

10 Discuss generalized analysis of transistor amplifier model using h-parameters.

OR

11 Discuss generalized analysis of FET amplifier model using small signal model.

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