

B.Tech II Year I Semester (R15) Regular Examinations November/December 2016

SWITCHING THEORY & LOGIC DESIGN

(Common to ECE and EIE)

Time: 3 hours

Max. Marks: 70

PART – A

(Compulsory Question)

- 1 Answer the following: (10 X 02 = 20 Marks)
- State De Morgan's theorem.
 - Reduce $A(A + B)$.
 - What is a prime implicant?
 - State the limitations of Karnaugh map.
 - Define combinational logic.
 - What is priority Encoder?
 - Define Flip flop.
 - Define race around condition.
 - Define address and word.
 - List the major differences between PLA and PAL.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

- 2 (a) Reduce $AB + (AC)' + AB'C$ ($AB + C$).
 (b) List Boolean laws and their Duals.

OR

- 3 (a) Convert the given expression in to canonical SOP form $Y = AC + AB + BC$.
 (b) Realize NOT, OR, AND gates using universal gates.

UNIT – II

- 4 (a) Explain with an example, four variable K map.
 (b) Minimize the following function and implement using AOI logic function : $F(A,B,C,D) = \prod(0,2,4,8,9,12,14)$.

OR

- 5 (a) Simplify using Tabular method: $Y(A,B,C,D,E) = \sum(2,3,5,7,10,12,13)$.
 (b) Minimize the following function: $F(A,B,C,D,E) = \sum(0,2,4,6,9,13,21,23,25,29,31)$.

UNIT – III

- 6 (a) Explain the function of an encoder and list its applications.
 (b) Design a Half adder using basic gates and explain its truth table.

OR

- 7 (a) With a neat diagram explain the operation of multiplexer.
 (b) Explain the function of Digital magnitude comparator using a neat diagram.

UNIT – IV

- 8 (a) Draw the logic diagram of a JK flip flop and using excitation table, explain its operation.
 (b) Design a 4-bit Binary ripple down-counter using a negative edge triggered D flip-flops.

OR

- 9 (a) Design a synchronous mod-6, counter with the following sequence: 5, 6, 7, 8, 9, 10, 5.....
 (b) Explain the difference between synchronous and asynchronous sequential circuits.

UNIT – V

- 10 (a) Explain the operation of RAM with suitable diagram.
 (b) Explain the features of flash memory.

OR

- 11 (a) Explain EEPROM with diagram.
 (b) With a neat figure, explain the features of PLA.
