Code: 15A04306 **R15**

B.Tech II Year I Semester (R15) Regular Examinations November/December 2016

DIGITAL LOGIC DESIGN

(Common to CSE and IT)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) What is the Gray equivalent of $(652)_{10}$?

(b) Simplify the Boolean expression F = (ABC)' + (AB)'C + A'BC' + A(BC)' + AB'C.

(c) What is a decoder? Draw the logic circuit of a 2 line to 4 line decoder.

(d) Compare PROM, PLA & PAL.

(e) What is problem of lock out in counters?

(f) Distinguish between latch & flip flop.

(g) Why multiplexer is called data selector?

(h) Convert JK Flip flop to T Flip flop.

(i) Define the following characteristics of digital logic families: (i) Propagation delay. (ii) Noise Margin.

(j) A 4-bit ripple counter and a 4-bit synchronous counter are made using flip flops having a propagation delay of 10ns each. What is the worst case delay in the ripple counter and the synchronous counter?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Perform $N_1 + N_2$, $N_1 + (-N_2)$ for the following numbers expressed in 2's complement representation. Verify answers by using decimal addition and subtraction.

$N_1 = 10001110$ $N_2 = 00001101$

(b) Simplify the following Boolean expressions to a minimum number of literals:

(i) (A'+C)(A'+C')(A'+B+C'D)

(ii) x'y' + xy + x'y

(c) Implement the following function using only NOR gates: F = a(b + cd) + bc'.

OR

3 (a) What is Hamming code? Test the following hamming code sequence for 11-bit message and correct it if necessary: (101001011101011).

(b) Reduce the expression f = A[B+C'(AB+AC')'].

(c) Express the Boolean function f = A(A'+B)(A'+B+C') to maxterms.

UNIT – II

4 (a) Reduce the following expressing using k-map: f = ∑m(1,3,4,5,8,9,13,15).

(b) Obtain minimal POS expression for $\Pi_M(1,2,3,8,9,10,11,14)$ d(7,15).

OR

5 (a) Implement the following function with NAND – AND and NOR – OR two level forms:

F = ∑m(0,1,2,3,4,8,9,12)

(b) Obtain minimal expression for f = ∑m(1,2,3,5,6,7,8,9,12,13,15) using the tabular method.

UNIT – III

6 (a) Design a combinational circuit with three inputs A, B and C and three outputs x, y and z. When the binary inputs are 0, 1, 2 and 3, the binary output is one greater than the input. When the binary inputs are 4, 5, 6 and 7 the binary outputs are one less than the input.

(b) Distinguish between an encoder and a priority encoder? Design an octal to binary priority encoder.

OR

7 (a) Briefly explain the operation of a carry look ahead adder

(b) Realize the function using F (A,B,C,D) = ∑m(0,1,2,5,9,14,13,15) using 8:1 MUX.

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UNIT – IV

8 (a) Draw the schematic circuit of an positive edge triggered JK Flip flop and explain its operation with the help of the truth table. How is the race around condition eliminated?

(b) Design a divide by 6 counter using T- flip flop. Write the state table and reduce the expressions using K – Map.

OR

9 (a) Design a clocked sequential machine using JK flip flop for the following state table diagram. Use the state reduction procedure if possible.

PS	NS, Z	
	X=0	X=1
A	A,0	B,0
B	C,0	B,0
C	A,0	B,1
D	A,0	B,0

(b) Distinguish between asynchronous and synchronous counters. Write the design steps of synchronous counters.

UNIT – V

10 (a) Implement a BCD to Gray code converter using ROM.

(b) Explain about basic circuit and NOR of ECL with its characteristics.

OR

11 (a) Implement the following Boolean function using PLA:

$F_1(A,B,C) = \sum m(3,5,6,7)$

$F_2(A,B,C) = \sum m(0,2,4,7)$

(b) Draw the circuit of CMOS two input NAND and NOR gate and explain its operation.

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