Code: 15A04503

R15

B.Tech III Year I Semester (R15) Supplementary Examinations June 2018

LINEAR INTEGRATED CIRCUITS & APPLICATIONS

(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) List the characteristics of an ideal op-amp.
(b) Sketch the equivalent circuit of an op-amp.
(c) Define slew rate.
(d) List the need for compensating networks.
(e) Sketch an adder circuit using op-amp to obtain the sum of three inputs.
(f) Sketch the op-amp differentiator circuit and write the output equation.
(g) Mention the applications of a Schmitt trigger circuit.
(h) List the basic building blocks of the PLL.
(i) Compare weighted resistor and R-2R ladder DAC.
(j) Give the principle of operation of flash ADCs.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Draw the circuit of basic current mirror and explain its operation.
(b) With block diagram, explain the general stages of an Op-Amp IC.

OR

3 Describe with diagrams, the open loop configurations of an op-amp.

UNIT – II

4 Explain in detail the voltage series, voltage shunt feedback circuits using op-amps.

OR

5 (a) Explain the open loop frequency response characteristics of an op-amp.
(b) Explain the frequency response characteristics of internally compensated op-amp.

UNIT – III

6 (a) Describe the circuit of a current to voltage converter circuit.
(b) Explain the circuit diagram of an integrator and derive its output equation.

OR

7 Describe with diagram, the working principle of an instrumentation amplifier.

UNIT – IV

8 With circuit diagram, describe the working of a Wien bridge oscillator circuit using op-amp.

OR

9 Draw the circuit of a monostable multivibrator using 555 IC and explain its operation.

UNIT – V

10 (a) Draw the circuit and explain the working of dual slope A/D converter.
(b) For a particular dual slope ADC, t_1 is 1ms and the reference voltage is -1V. Calculate t_2 if V_1 is 5 V and RC time constant is 1 msec.

OR

11 Describe the operation of high speed sample and hold circuits.

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