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C20-AEI–303

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BOARD DIPLOMA EXAMINATION, (C-20)

OCTOBER/NOVEMBER—2023

DAEIE – THIRD SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 Hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed five simple sentences.

1. Add $(1010101)_2$ and $(111101)_2$ using binary addition.

2. State De-Morgan's theorems.

3. State the importance of parity bit.

4. Distinguish between serial and parallel adder in any three aspects.

5. List any three applications of decoder.

6. Draw 4-bit parallel adder using full adders.

7. State the race around condition.

8. Define counter.

9. State the need for a register.

10. Define the terms 'resolution' and 'monotonicity' of D/A converter.

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PART—B

8×5=40

Instructions : (1) Answer **all** questions.

(2) Each question carries **eight** marks.

(3) Answers should be comprehensive and criterion for valuation is the content but not the length of the answer.

11. *(a)* Explain any four postulates in Boolean algebra. Draw the symbols of AND, NOT gates with truth tables.

(OR)

(b) Explain the working of NAND and NOR gates using truth tables.

12. *(a)* Explain one-bit digital comparator with a diagram.

(OR)

(b) Draw and explain 2's compliment parallel adder/subtractor circuit.

13. *(a)* Draw and explain JK master slave flip-flop with truth table.

(OR)

(b) Draw and explain the working of ring counter and list any two applications.

14. *(a)* Explain the principle of working of ROM.

(OR)

(b) Explain the working of shift left and shift right registers with a diagram.

15. *(a)* Explain D/A conversion using weighted resistors with a diagram.

(OR)

(b) Explain A/D conversion using successive approximate method with a diagram.

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PART—C

10×1=10

Instructions : (1) Answer the following question.

(2) The question carries **ten** marks.

(3) Answer should be comprehensive and the criterion for valuation is the content but not the length of the answer.

16. Realize half adder using NAND gates only and NOR gates only.

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