C20-BM–**304**

7222

BOARD DIPLOMA EXAMINATION, (C-20)

OCTOBER/NOVEMBER—2023

DBME - THIRD SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 Hours]

[*Total Marks* : 80

PART—A

3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed five simple sentences.

1. State De-Morgan's theorem.

2. Define the truth tables of NAND and NOR gates.

3. Draw half-adder circuit using an Ex-or gate.

4. Compare serial adder with parallel adder.

5. Construct full adder using 3x8 decoder.

6. Define edge triggering in flip-flops.

7. Write the use of shift registers as memory.

8. State any three applications of counters.

9. Define word length and access time.

10. Classify different types of memories.

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Instructions : (1) Answer **all** questions.

(2) Each question carries **eight** marks.

(3) Answers should be comprehensive and criterion for valuation is the content but not the length of the answer.

11. *(a)* Draw an open collector TTL NAND gate and explain its working.

(OR)

(b) Compare the performance of TTL gate with respect to CMOS gate.

12. *(a)* Explain 4-bit parallel adder and 2's compliment subtractor with circuit.

(OR)

(b) Compare serial adder with parallel adder and design a 4 to 2 line priority encoder.

13. *(a)* Explain the working of a RS-flip-flop with truth table.

(OR)

(b) Explain the working of NAND/NOR gate latch.

14. *(a)* Explain the circuit of a decade counter with wave form and truth table.

(OR)

(b) Draw the 4-bit ring counter circuit and explain its operation.

15. *(a)* Explain the concept of touch screen display and list the advantages of LED display with LCD display.

(OR)

(b) Compare the advantages and disadvantages of dynamic RAM over static RAM.

PART—C

Instructions : (1) Answer the following question.

(2) The question carries **ten** marks.

(3) Answer should be comprehensive and the criterion for valuation is the content but not the length of the answer.

16. Can the selection of JK flip-flop in digital circuits be replaced with RS flip-flop? Justify your answer.

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