Code No: 113AU **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, March - 2017
ELECTRONIC DEVICES AND CIRCUITS
(Common to EEE, ECE, CSE, EIE, IT, MCT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) Explain the Space charge region. [2]
b) Explain the operation of p-n junction biased in the reverse direction. [3]
c) Define Peak Inverse Voltage. [2]
d) Explain the harmonic components in rectifier. [3]
e) Write the complete expression for IC for any VC and IE. [2]
f) Explain the basewidth modulation. [3]
g) Why a capacitive coupling used to connect signal source to an amplifier. [2]
h) Explain the thermal instability. [3]
i) What is Pinchoff Voltage? [2]
j) Define transconductance gm and drain resistance of a FET. [3]

PART-B

(50 Marks)

2.a) Explain about the Current components in a p-n diode.
b) Sketch the piecewise linear characteristics of a diode. What are the approximate cutin voltages for silicon and germanium? [5+5]

OR

3.a) Obtain the static and dynamic resistances of the p-n junction germanium diode, if the temperature is 27^0 C and I_o=1μA for an applied forward bias of 0.2 V.
Assume =1.38×10^{-23} J/^{o}k.
b) Define diffusion and transition capacitance of p-n junction diode. Prove that diffusion capacitance is proportional to current I. [5+5]

4.a) Explain about L section Filters.
b) A full-wave single phase rectifier employs a pi- section filter consisting of two 4 μF capacitances and a 20 H choke. The transformer voltage to the center tap is 300 V rms. The load current is 500 mA. Calculate the dc output voltage and the ripple voltage. The resistance of the choke is 200Ω. [5+5]

OR

5.a) Draw and explain the Thevenin's model for Full-wave rectifier.
b) Explain the Voltage regulation using Zener Diode. [5+5]

6.a) Differentiate between NPN and PNP transistors.

b) Explain the input and output characteristics of the transistor in CC configuration with diagrams. How do you obtain from these? [3+7]

OR

7.a) Draw the circuit diagram of a pnp junction transistor in CE configuration and describe its characteristics.

b) Compare CB and CC configurations. [5+5]

8.a) Explain the DC and AC load Line analysis.

b) Draw and explain the Fixed Bias Circuit. Explain why the circuit is unsatisfactory if the transistor is replaced by another of same type. [5+5]

OR

9.a) Draw and explain the Voltage Divider Biasing.

b) Explain the Thermal runaway. [5+5]

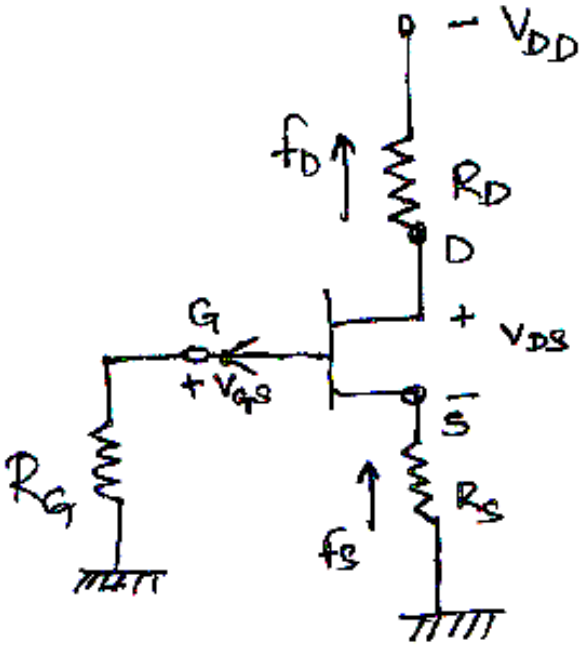
10.a) Explain the JFET Small signal Model.

b) Explain the MOSFET characteristics in enhancement mode. [5+5]

OR

11.a) Explain the FET Common Drain Amplifier.

b) A P-channel FET has V_P = 4V and I_{DSS} = 12mA. For the figure, determine R_D and R_S so that I_D=4 mA and V_{DS}=6V. V_{DD} is 12 V. [5+5]



---ooOoo---