Code No: 113BQ

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, March - 2017

DIGITAL LOGIC DESIGN AND COMPUTER ORGANIZATION

(Information Technology)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART-A

(25 Marks)

1.a)	Solve the Hexadecimal number 2456 into decimal number.	[2]
b)	Describe the steps involved in execution of a program.	[3]
c)	List all the basic logic gates and universal logic gates.	[2]
d)	Give the comparison between synchronous and asynchronous counter.	[3]
e)	Describe conditional jump with an example.	[2]
f)	Define about little-endian and big-endian.	[3]
g)	Describe paged segmentation.	[2]
h)	Explain the micro programmed control unit.	[3]
i)	List the advantages of DMA transfer.	[2]
j)	Write short notes on dual address cycle command.	[3]

PART-B

(50 Marks)

2.a) Discuss the operational concepts of a digital computer and explain the various types of computers and their applications.

b) Calculate the following to binary and then to gray code,
(i) 1001_{16} (ii) 7623_8 (iii) 1234_8 (iv) 1257_{10} (v) 2239_{10}. [5+5]

OR

3.a) Solve the number $(+542.5)_{10}$ as a floating point binary number with 24 bits the normalized fraction mantissa has 16 bits and the exponent has 8 bits.

b) Differentiate between RISC and CISC architectures. [5+5]

4.a) With a neat diagram explain parallel in parallel out shift register.

b) Solve the expression $Y=A\bar{B} + \bar{A}B$ using only 2 input NAND gates. [5+5]

OR

5.a) Solve the multi-level NAND circuit for the following expression
$F(A,B,C,D)= (A\bar{B} +C\bar{D})E+BC(A+B)$

b) Design a PAL for the following equation, $F= \bar{a}\ b\ c + \bar{b}\ c + ab$. [5+5]

6.a) With a neat diagram explain the floating point multiplication algorithm.

b) Explain the Addressing modes present in IA-32 Pentium processor. [5+5]

OR

7.a) What is a straight line sequencing and explain with an example.

b) Write the Booth's algorithm for multiplication of signed-2's complement numbers. [5+5]

8.a) Explain the organization of the control unit to allow conditional branching in the Microprogram.

b) Explain in detail the memory interleaving. [5+5]

OR

9.a) Give the timing diagram of a memory write operation and explain.

b) Show the control steps for the Branch-on-Negative instruction for a processor that has the three-bus structure. [5+5]

10.a) With a neat diagram explain the implementation of interrupt priority using individual interrupt request and acknowledgment lines.

b) Briefly summarize the bus signals of SCSI bus. [5+5]

OR

11.a) Explain in detail the DMA controller.

b) Explain the concept of the programmed I/O with a suitable example. [5+5]

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