Code No: 123BQ **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, November/December - 2016
DIGITAL LOGIC DESIGN AND COMPUTER ORGANISATIONS
(Information Technology)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) Write advantages of 4th Generations Computer. [2]
b) Convert the hexadecimal number 2AC5.D to binary and octal. [3]
c) What is race around condition? [2]
d) Implement AND logic using NAND gate. [3]
e) Write about IEEE 754 floating point format. [2]
f) Compare CISC and RISC architectures. [3]
g) What is Multiple Bus Organization? [2]
h) What is the difference between SRAM and DRAM? [3]
i) What is the need of Interface circuit. [2]
j) What is bus arbitration? Mention the types of bus arbitration. [3]

PART-B

(50 Marks)

2.a) Explain about communication topologies used in multiprocessors.
b) Perform the arithmetic operation (-638) + (+785) with the decimal numbers using signed 10's complement representation for negative numbers. [5+5]

OR

3.a) Solve for x
i) $(367)_8 = (x)_2$ ii) $(378.93)_{10} = (x)_8$
iii) $(B9F.AE)_{16} = (x)_8$ iv) $(16)_{10} = (100)_x$
b) Convert $(163.875)_{10}$ to binary, octal, hexadecimal. [5+5]

4.a) Explain the differences between a MUX and a DEMUX. Realize 16-input multiplexer by cascading of two 8-input multiplexers.
b) Draw the half adder circuit with equations. [6+4]

OR

5.a) What are universal gates? Realize AND, OR, NOT, XOR gates using universal gates.
b) Obtain the canonical SOP form of the following functions. [5+5]
i) Y(A,B) = A+B. ii) Y(A,B,C,D) = AB+ACD.

6. What is an addressing mode? Explain the different addressing modes with examples. [10]

OR

7.a) Discuss briefly the hardware implementation of Signed-Magnitude data.
b) Explain the Basic Machine Instructions. [5+5]

8.a) With a neat diagram explain the hard wired control circuit.
b) Explain the single bus multi-processor organization. [5+5]

OR

9.a) Discuss the address translation in the case of virtual memory diagrammatically.
b) Explain the cache memories. [5+5]

10.a) Explain the handshake control data transfer during input and output operation in asynchronous bus with timing diagram.
b) Explain USB addressing and protocols. [5+5]

OR

11.a) With necessary timing diagrams explain about synchronous and asynchronous buses.
b) Illustrate programmed I/O with an example. [5+5]