Code No: 123BQ **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, November/December - 2017
DIGITAL LOGIC DESIGN AND COMPUTER ORGANIZATION
(Information Technology)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) Convert following hexadecimal to decimal numbers. [2]
(i) $F28_{16}$ (ii) $BC2_{16}$.
b) Draw the different bus structures. [3]
c) What is code converter? [2]
d) Explain the design procedure of combinational circuit. [3]
e) Write about IEEE 754 floating point format. [2]
f) Explain with simple example fixed point addition. [3]
g) Define: i) Hit ratio ii)Virtual memory. [2]
h) List out the characteristics of secondary storage. [3]
i) What is the need of Interface circuit? [2]
j) Write short note on DMA. [3]

PART-B

(50 Marks)

2.a) Compare different Computer Generations.
b) Write a short note on Gray codes, Excess-3 codes. [5+5]

OR

3.a) Explain about multiprocessors and multi computers.
b) Discuss about functional units of basic computer. [5+5]

4.a) What are universal gates? Realize AND, OR, NOT, XOR gates using universal gates.
b) Draw and Explain about SR flip flops and D flip flops. [5+5]

OR

5.a) Draw and explain about shift register in-detail.
b) Draw the half adder circuit with equations. [5+5]

6.a) Discuss briefly the hardware implementation of Signed - Magnitude data.
b) Explain the Basic Machine Instructions. [5+5]

OR

7.a) Explain various instructions present in IA-32 Pentium processor.
b) Discuss about Hardware Implementation of arithmetic and logic operations. [5+5]

8.a) Briefly explain about memory management requirements.

b) Differentiate between hard wired and micro programmed control unit. [5+5]

OR

9.a) Discuss about the concept of cache memory.

b) Discuss the address translation in the case of virtual memory diagrammatically. [5+5]

10.a) Explain USB addressing and protocols.

b) Explain the handshake control data transfer during input and output operation in asynchronous bus with timing diagram. [5+5]

OR

11.a) Explain how interrupts are handled from multiple devices.

b) Explain the SCSI bus standard. [5+5]

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