JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

# B.Tech II Year I Semester Examinations, April/May - 2018 DIGITAL LOGIC DESIGN 

(Common to CSE, IT)
Time: 3 Hours
Max. Marks: 75

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have $\mathrm{a}, \mathrm{b}, \mathrm{c}$ as sub questions.

## PART- A

1.a) Convert (67A9) ${ }_{16}$ into decimal.
(25 Marks)
b) Add (+80) and ( -70 ) using 2 's complement.
c) Write the truth table of Ex-OR Gate.
d) Implement OR gate using NAND gates only.
e) Write the truth table of half adder.
f) Design half sub tractor circuit.
g) Differentiate between Latch and flip flop.
h) Draw the circuit diagram of Ring counter.
i) Differentiate between RAM and ROM.
j) Name any 3 logic micro operations.

## PART-B

(50 Marks)
2.a) i) Convert (657) $)_{8}$ into decimal.
ii) Convert (2348) $)_{10}$ into hexa decimal.
b) Represent the decimal number 46.5 as a floating point number with 16 bit mantissa and 8 bit exponent.

## OR

3.a) i) Convert 110001.1010010 into hexadecimal.
ii) Convert (423.25) ${ }_{10}$ into Hex.
b) i) Simplify $A(B+C)+A B+A B C$
ii) Write the truth table and symbols of AND and OR gates.
4. Obtain the simplified expression in sum of products for the following Boolean function.
a) $\mathrm{F}(\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D})=\sum(2,3,12,13,14,15)$;
b) $\mathrm{BDE}+\mathrm{B}^{\prime} \mathrm{C}^{\prime} \mathrm{D}+\mathrm{CDE}+\mathrm{A}^{\prime} \mathrm{B}^{\prime} \mathrm{CE}+\mathrm{A}^{\prime} \mathrm{B}^{\prime} \mathrm{C}+\mathrm{B}^{\prime} \mathrm{C}^{\prime} \mathrm{D}^{\prime} \mathrm{E}^{\prime}$

OR
5. Obtain the simplified expression in product of sums.
a) $\mathrm{F}(\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D})=\pi(0,1,2,3,4,10,11)$
b) $\mathrm{F}(\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D})=\pi(1,3,5,7,13,15)$
6.a) Design half adder using only NAND gates.
b) Design a combinational circuit which converts BCD to Excess- 3 code.
7.a) Design a 2 bit magnitude comparator.
b) Implement $4 * 16$ decoder using two $3 * 8$ decoders.
8.a) Explain a right shift register.
b) Design a 3 bit Ripple counter.

## OR

9.a) What is a hazard? How do you eliminate hazards?
b) Design and explain Johnson counter.
10.a) Explain different types ROMs.
b) Implement the following Boolean functions using PLA with 3 AND gates. $\mathrm{F}_{1}(\mathrm{ABC})=\sum(3,5,7), \quad \mathrm{F}_{2}=\sum(4,5,7)$.

OR
11.a) Explain the applications of Logic micro operations.
b) Explain shift Right and Left with examples.

