Code No: 133AJ **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, November/December - 2017
DIGITAL LOGIC DESIGN
(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) Subtract the following using 1's and 2's complement $(101)_2$ - $(10110)_2$. [2]
b) Distinguish between canonical and standard forms by giving an example. [3]
c) Derive the sum of minterms for the function f(a,b,c)=a′b+b′c′ [2]
d) Implement the following function using only NAND Gates F=a.(b′+ c′) + (b. c). [3]
e) Differentiate multiplexer and de-multiplexer. [2]
f) Draw the diagram of 4-Bit Parallel adder cum parallel subtractor. [3]
g) Show the excitation table and truth table of JK flip flop. [2]
h) Differentiate critical and non-critical race. [3]
i) Define Register Transfer Language. [2]
j) Differentiate PLA and PAL. [3]

PART-B

(50 Marks)

2.a) What are the various logic gates, give the representation along with the truth table.
b) What is the use of complements? Perform subtraction using 7's complement for the given Base-7 numbers (565)-(666). [5+5]

OR

3.a) Convert the following to the corresponding bases
i) $(9BCD)_{16}$ = ( )$_8$
ii) $(323)_4$ = ( )$_5$
b) Given the 8 bit data word 11011011, generate the 12 bit composite word for the Hamming code that corrects and detects single errors. [5+5]

4.a) Derive the product of maxterms for f(a,b,c,d)=a.b.c+ b′.d+c.d′.
b) Derive and Implement Exclusive OR function involving three variables using only NAND function. [5+5]

OR

5.a) Obtain the simplified expression in SOP form of F(a,b,c,d,e)=∑(1,2,4,7,12,14,15,24,27,29,30,31)using K-maps.
b) Implement the function f(a,b,c)=π(0,1,3,4) using NAND-NAND two level gate structure. [5+5]

6.a) Implement and odd parity generator for 3-bit using a decoder.

b) Design a circuit for 2-bit binary multiplier. [5+5]

OR

7.a) Define a multiplexer? Draw a 4:1 multiplexer for the function
$f(a,b,c,d)=\sum(0, 4,5,10,11,12,15)$

b) Design a full binary adder with two half adders and a OR gate. [5+5]

8.a) Explain about a NOR Latch in detail, with a neat diagram.

b) Design a 3-bit counter using T flip flops. [5+5]

OR

9. Define essential hazard? Implement SR Latch by avoiding Hazard Neatly draw the diagram of SR latch before hazard and after Hazard elimination. [10]

10. Explain about RAM in detail. [10]

OR

11. What is a micro operation? List and explain its categories with relevant examples. [10]

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