Code No: 133AJ **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, December - 2019
DIGITAL LOGIC DESIGN
(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) Convert $(10110)_2$ to Gray code and $(110101)_G$ to binary number. [2]
b) Explain about Floating point number representation with an example. [3]
c) What are universal gates and why they are called as universal gates. [2]
d) Realize the following function as multilevel NAND-NAND network
$f = B(A + CD) + A\bar{C}$ [3]
e) What is a multiplexer? What is the function of a multiplexer's select input. [2]
f) Can more than one decoder output be activated at one time? Justify your answer? [3]
g) What is a flip-flop? Write down the characteristic equation of S-R flipflop. [2]
h) Discuss the difference between synchronous and asynchronous sequential circuits. [3]
i) What are shift micro operations and what are the different types. [2]
j) Explain about sequential programmable logic devices [3]

PART-B

(50 Marks)

2.a) Convert the following
i) $(53.625)_{10}$ to (? $)_2$ ii) $(3FD)_{16}$ to (? $)_2$ iii) $(A69.8)_{16}$ to (? $)_{10}$
b) Perform the decimal subtraction in 8-4-2-1 BCD using 9's complement
i) Subtract 79 from 26 ii) Subtract 748 from 983. [5+5]

OR

3.a) Simplify the following expression using Boolean algebra rules $\overline{\overline{A\bar{B} + ABC} + A(B + A\bar{B})}$
b) Check whether the received code 10101100 is correctly received or not if even parity is used. [5+5]

4.a) Reduce the following function using K-Map.
F(A,B,C,D,E) = Σm(1,4,8,10,11,20,22,24,25,26)+d(0,12,16,17)
b) Write down the procedure to convert a given AND-OR gate network to all NAND gate network and illustrate with an example. [5+5]

OR

5.a) Obtain the minimal sum of products expression for the following function and implement the same using only NAND gates
$f(A,B,C,D) = \sum(1,4,7,8,9,11) + \Sigma_d(0,3,5)$
b) Realize the following function with i) Multilevel NAND-NAND network and
ii) Multilevel NOR-NOR network.
$Y = \bar{A}B + B(C + D) + E\bar{F}(\bar{B} + \bar{D})$ [5+5]

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6.a) What is a combinational logic circuit? Implement a Full adder using two half adders and one OR gate.

b) With a neat diagram explain in detail about Decimal Adder. [5+5]

OR

7.a) Design and explain a 4-bit binary parallel Adder/Subtractor.

b) Draw the logic diagram of 2:4 Decoder with an ENABLE input using: i) NAND gates ii) NOR gates. Show that the realization using NAND gates is more convenient to distinguish the selected output with a value of 0. [5+5]

8.a) Convert an SR Flip-Flop into JK Flip-Flop.

b) With a neat diagram explain about 4-bit bidirectional shift register. [5+5]

OR

9. Design the counter that goes through states 1,2,4,5,7,8,,10,11,1.....using JK flip-flops. [10]

10.a) A combinational circuit is defined by the functions:

$F_1 = \sum m(3,5,7)$ $F_2 = \sum m(4,5,7)$

Implement the circuit with a PLA having 3 inputs, 3 product terms and two outputs.

b) Explain about Read and Write cycles of a static RAM with neat timing waveforms. [5+5]

OR

11. With a neat diagram explain in detail about two dimensional memory decoding scheme. [10]

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