Code No: 134AK **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, May - 2019
COMPUTER ORGANIZATION
(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	What is the purpose of BUN instruction?	[2]
b)	Define computer organization, computer architecture.	[3]
c)	Contrast 8086 minimum mode with maximum mode.	[2]
d)	How an address is latched in 8086?	[3]
e)	What is the need of a linker?	[2]
f)	What is the difference between a macro and a procedure?	[3]
g)	What is the disadvantage of strobe method?	[2]
h)	Provide the hardware for signed-2's complement addition and subtraction.	[3]
i)	Define miss penalty for cache memory.	[2]
j)	Draw the system bus structure for multiprocessors.	[3]

PART – B

(50 Marks)

2. List the registers for the basic computer and give their functionality in program execution. [10]

OR

3. Describe the micro programmed control organization and compare its advantages over hardwired control. [10]

4. Evaluate the following arithmetic statement using zero, one, two and three address instructions. Use the conventional symbols and instructions.
X = (A+B) * (C+D). [10]

OR

5. Does 8086 support instruction pipelining? Justify your answer with relevant example instructions. [10]

6. Develop an assembly language program to find out numbers odd and even numbers in a given series of 16-bit hexa decimal numbers. [10]

OR

7. Elaborate on the techniques used to pass parameters to procedures in assembly language program. [10]

8. Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. (+33) × (-12). [10]

OR

9. Design a circuit for a 4 × 4 First In First Out Buffer and explain its functionality. [10]

10. A digital computer has a memory unit of 64K * 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of 4 words.
(a) How many bits are there in the tag, index, block and word fields of the address format?
(b) How many bits are there in each word of cache and how are they divided into function? Include a valid bit. [10]

OR

11. Does pipelining get affected by data dependencies among the instruction? Justify your answer with lucid examples. [10]

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