Code No: H6802/R13

M. Tech. II Semester Regular/ Supplementary Examinations, July-2016

CMOS MIXED SIGNAL CIRCUIT DESIGN

(Common to VLSI & ES, ES & VLSI, VLSID & ES, ES & VLSID, VLSI, VLSID, VLSISD and VLSI & ME)

Time: 3 Hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1.	a	Explain the non-ideal characteristics of a switchedcapacitor integrator.	6
	b	For the above circuit, if clock frequency is 100kHz, find the capacitor value that will emulate 1M ohm resistor.	6
2.	a	Derive an integrator using switched capacitor circuit.	6
	b	Explain the techniques that are adopted in a switched capacitor integrator circuit to minimize charge injection issues.	6
3.	a	Explain the basic charge pump PLL and non-ideal effects in PLLs.	6
	b	Explain the Jitter in PLLs and delay locked loops.	6
4.		Mention all kinds of medium speed and high speed ADC and explain the operation of a multiple-bit pipeline ADC.	12
5.	a	Design a thermometer code charge redistributionD/A converter.	8
	b	Write about hybrid converters.	4
6.		Explain about deterministic approach and statistic approach of quantization noise in data converters.	12
7.	a	What is a flash converter? Discuss the working of a 3-bit flash A/D Converter.	6
	b	Design a 3-bit Flash ADC with quantization error centered about zero LSBs.	6
8.		Distinguish oversampling without noise shaping and with noise shaping.	12

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