Code No: I6803/R16

M. Tech. I Semester Regular/Supple Examinations, Jan/Feb -2018

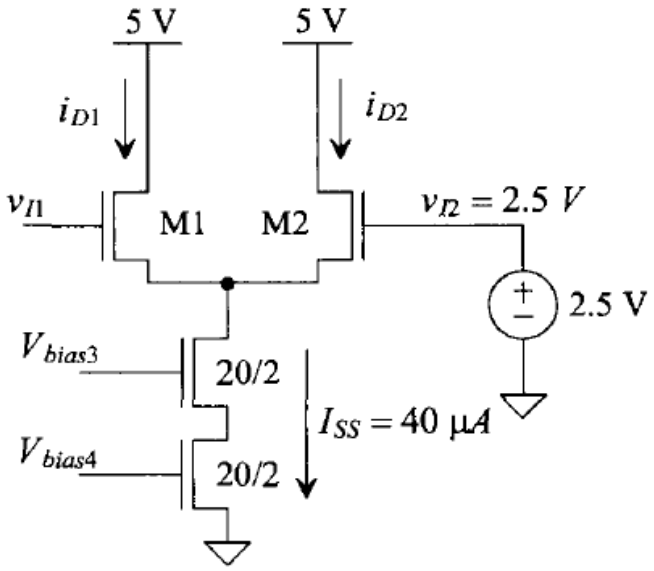
CMOS ANALOG IC DESIGN

Common to VLSI&ES (68), ES&VLSI (48), VLSID &ES (77), ES &VLSID (81), VLSI (57), VLSID (72), VLSI System Design (61), VLSI & Micro Electronics (76)

Time: 3 Hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1.	a	Write a brief note on various passive components that are available in CMOS technologies with relevant diagrams	8M
	b	With necessary schematics, explain the term Latch up in CMOS Technology	4M
2.	a	Draw the model for a non ideal switch and explain its parameters in detail	5M
	b	Draw and explain about a simple current mirror with Beta helper.	7M
3.	a	Draw and explain the circuit diagram for voltage reference with high sensitivity	5M
	b	Explain the Inverter DC characteristics and also give your inference on MOSFET channel length	7M
4.	a	With relevant expressions explain the terms maximum and minimum differential i/p voltage	6M
	b		6M



Estimate the maximum and minimum voltage on the gate of Ml in Fig. that ensures that neither Ml or M2 shut off.(Assume the necessary data)

5.		With the necessary schematics explain the following terms	
		i) Simple folded cascode	4M
		ii) Folded cascode with biasing	4M
		iii) Folded cascode with nMOS input	4M
6.	a	With a schematic explain about operational-amplifier with its equivalent circuit	4M
	b	Define and explain the following terms i) Common-Mode Input Range ii) Common-Mode Rejection Ratio	8M
7.	a	Draw the schematic for a Folded-cascode op-amp with class AB output buffer and explain its operation	6M
	b	Draw the Block diagram of a spectrum analyzer and explain the procedure to measure the spectral content of a signal	6M
8.	a	Write a note on characterization of comparator	5M
	b	With relevant schematics explain about discrete-time comparators.	7M

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