Code No: I6803/R16

M. Tech. I Semester Supplementary Examinations, February -2020

CMOS ANALOG IC DESIGN

Common to VLSI&ES (68), ES&VLSI (48), VLSID &ES (77), ES &VLSID (81), VLSI (57), VLSID (72), VLSI System Design (61) and VLSI & Micro Electronics (76)

Time: 3 Hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1.	a	Explain the various model parameters in MOS.	6M
	b	Discuss about the computer simulation models	6M
2.	a	Using small signal analysis, Derive an expression for the output resistance of the cascode current source	6M
	b	Explain about the current mirror with degeneration helper with equations	6M
3.	a	Explain class A output amplifier.	6M
	b	With derivation explain the operation of single ended input current amplifier.	6M
4.	a	Explain the procedure for the design of an op-amp.	6M
	b	Derive an expression for slew rate of a cmos op-amp.	6M
5.	a	Explain the circuit of a switched capacitor comparator.	6M
	b	Explain the operation of push-pull output comparator.	6M
6.	a	Explain any two of the op-amp compensation techniques.	6M
	b	Define and drive an expression for threshold voltage of a MOS.	6M
7.	a	With necessary circuit explain the current and voltage references.	6M
	b	Explain the operation of MOS switch.	6M
8.		Write short notes on the following	
	a	Open loop comparator	6M
	b	Cascode Op-amp	6M

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