Code No: **R32052**　　　　**R10**　　　　Set No. 1

**III B.Tech II Semester Supplementary Examinations, April – 2017**
**COMPUTER ARCHITECTURE**
**(Computer Science Engineering)**

Time: 3 hours　　　　　　　　　　　　　　　　　　　　Max. Marks: 75

**Answer any FIVE Questions**
**All Questions carry equal marks**
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1　Describe at least four characteristics of MIMD multiprocessor that distinguish them　[15M]
　　from multiple computer systems or computer networks.

2　a)　Draw and explain the memory hierarchy for personal mobile devices.　[8M]

　　b)　Write a short note on Virtual Memory and Virtual Machines.　[7M]

3　a)　Make a comparison between the typical RISC and typical CISC processor　[10M]
　　　　architectures.
　　b)　Explain about Instruction-set Architectures.　[5M]

4　a)　Define latency. Explain Collision with scheduling latency.　[7M]

　　b)　Give a brief note on Instruction Execution Phases.　[8M]

5　a)　Explain the principles of vector processing.　[7M]

　　b)　Discuss the Cray Y-MP Multi vector Multiprocessors.　[8M]

6　a)　Briefly explain the Bus-Snooping Cache Coherence Protocols.　[7M]

　　b)　Discuss the Directory-based cache coherence**.**　[8M]

7　a)　Explain MIMD with distributed Memory with a neat diagram.　[7M]

　　b)　List and explain MIMD design Issues.　[8M]

8　a)　Write a short note on Complexity of PRAM Algorithms.　[7M]

　　b)　Discuss about the Cray Line of Computer Systems.　[8M]

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