Code No: **R32052** **R10** **Set No. 1**

III B.Tech II Semester Regular/Supplementary Examinations, May/June - 2015
COMPUTER ARCHITECTURE
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
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1 a) Make a comparison of first five generations of electronic computers. [8]
b) Explain Flynn's classification. [7]

2 a) Where can be a block placed in a cache? Discuss the three categories of cache organization. [10]
b) How to compute average memory access time? [5]

3 a) Explain the design space of modern processor families with a neat diagram. [8]
b) Give the architecture of the MC68040 processor. [7]

4 a) Make a comparison of a synchronous pipeline model and an asynchronous pipeline. [8]
b) Explain dynamic instruction scheduling. [7]

5 a) Describe the schematic design of a cross point switch in a crossbar network. [8]
b) Explain routing in butterfly networks. [7]

6 Discuss cache coherence problems in data sharing and in process migration. Explain any one protocol approach for handling this problem. [15]

7 a) Write about the NEWS grid of CM-2 and explain scanning and spread mechanism. [7]
b) Explain the functionality of the processing node in the CM-5 system. [8]

8 How to improve performance of a system with parallel processing? Explain with illustrations. Give a brief overview of trends in parallel systems. [15]

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Code No: **R32052** **R10** **Set No. 2**

III B.Tech II Semester Regular/Supplementary Examinations, May/June - 2015
COMPUTER ARCHITECTURE
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

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1	a)	Discuss the elements of a modern computer system in the context of parallel processing	[8]
	b)	Describe the COMA model of a multiprocessor.	[7]
2	a)	"Virtual memory increases the performance of the system" – support this statement with proper explanation.	[7]
	b)	Discuss the merits and demerits of multi level caches.	[8]
3	a)	Discuss the distinction between typical RISC and typical CISC processor architectures.	[8]
	b)	Explain the locality property and its three dimensions.	[7]
4	a)	Explain pipeline schedule optimization techniques	[8]
	b)	Discuss hardware score boarding for dynamic instruction scheduling.	[7]
5	a)	Explain routing in omega network.	[7]
	b)	Describe modular construction of butterfly switch networks with 8X8 cross bar switches.	[8]
6	a)	Explain snoopy bus protocol for cache coherence.	[7]
	b)	Discuss the concept of virtual channel. What is its role in avoiding deadlocks?	[8]
7		Describe the distributed memory model and shared memory models for constructing SIMD supercomputers.	[15]
8	a)	Make a comparison of instruction level parallelism and structural parallelism.	[8]
	b)	Explain any one parallel algorithm in detail.	[7]

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Code No: **R32052** **R10** **Set No. 3**

III B.Tech II Semester Regular/Supplementary Examinations, May/June - 2015
COMPUTER ARCHITECTURE
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
*****

1 a) Describe the architectural evolution of computer systems. [9]
b) Explain the six layers for computer system development. [6]

2 a) Which block should be replaced on a cache miss? Explain any two strategies in detail. [9]
b) Compare and contrast paging with segmentation [6]

3 a) Describe the architectural model of a basic scalar computer system. [8]
b) Give the SPARC architecture with the processor and the floating point unit. [7]

4 a) Discuss the usage of the following buffers
(i)sequential buffer (ii)target buffer (iii)loop buffer [9]
b) What is a reservation table? Discuss its need in a pipeline. [6]

5 a) What is hot spot problem? Explain with an example. [6]
b) How to build 8 X 8 omega network with 2 X 2 switches? Explain with a neat diagram. [9]

6 a) Explain directory based protocol for cache coherence. [7]
b) Discuss various communication patterns in multicomputer networks. [8]

7 a) Describe the architecture of the CM-2 system [7]
b) What are permutation operations for inter processor communications on the CM-5 system? Explain with suitable diagrams. [8]

8 Explain parallel processing techniques used in Cray Line of computer systems. [15]

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Code No: **R32052** **R10** **Set No. 4**

III B.Tech II Semester Regular/Supplementary Examinations, May/June - 2015
COMPUTER ARCHITECTURE
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
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1	a)	How to measure the performance of a computer system? Explain with examples.	[8]
	b)	Discuss the operational model of SIMD computers.	[7]
2		Discuss in detail the basic cache optimizations for improving cache performance.	[15]
3	a)	Compare the main features of RISC and CISC processors	[8]
	b)	State the inclusion property and explain the data transfers between adjacent levels of a memory hierarchy.	[7]
4	a)	What are the possible hazards in an instruction pipeline? Quote examples.	[8]
	b)	Does a pipeline improve system's performance? Justify your answer.	[7]
5	a)	Explain the broad cast capability of an Omega network built with 4 X 4 switches.	[8]
	b)	Describe multiport memory organizations for multiprocessor systems.	[7]
6	a)	Compare and contrast full-map directories with limited directories.	[8]
	b)	Describe adaptive X-Y routing using virtual channels.	[7]
7		Discuss the building blocks and the application paradigms of CM-5 machine.	[15]
8	a)	Discuss the instruction level parallelism and its limitations.	[7]
	b)	Explain stream processing as a parallel application.	[8]

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