Code No: **R32052** **R10** **Set No. 1**

III B.Tech II Semester Supplementary Examinations, November/December – 2016

COMPUTER ARCHITECTURE

(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1	a)	Distinguish between Multiprocessors and Multi-computers.	[7M]
	b)	Briefly explain about Shared Memory Multiprocessors.	[8M]
2	a)	Draw and explain the memory hierarchy for server.	[7M]
	b)	"Caches are used to reduce Hit time & Power" – support this statement with suitable example.	[8M]
3		Draw and explain four-level memory hierarchy with increasing capacity and decreasing speed and cost from low to high levels.	[15M]
4	a)	Explain the Complexity of Link Scheduling.	[7M]
	b)	Discuss the linear Pipeline Processors with an example.	[8M]
5	a)	Explain the Multistage Crossbar Network in the Cray Y-MP 816.	[7M]
	b)	What are the various physical forms available for establishing an interconnection network? Explain.	[8M]
6	a)	Explain the Cache Coherence in Shared Memory Multiprocessors.	[7M]
	b)	Give a brief note on Flow Control Strategies.	[8M]
7	a)	Discuss the Synchronized MIMD Machine.	[7M]
	b)	Explain the Inter processor Communications.	[8M]
8	a)	Briefly explain the trends in Parallel Systems.	[7M]
	b)	Explain about stream processing in Cray- line computers.	[8M]

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