[Total No. of Questions: 12]

S.E. (E&TC/ Electronics)

DIGITAL ELECTRONICS

(204185) (2012 Course)

Time : 2 Hours]

[Max. Marks : 50

Instructions to the candidates:

- 1) Attempt Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8, Q.9 or Q.10, Q.11 or *Q.12* .
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Assume suitable data, if necessary.
- 5) Use of logarithmic tables, slide rule and electronic non programmable calculator is allowed.

Q1	a.	Explain following characteristics of digital ICs				
		 Noise margin Fan in & Fan out 	02			
	b	Simplify and implement following expression using K-map.				
		$Y = \sum m (1,5,6,7,11,12,13,15)$	04			
	OR					
Q2	а	Draw CMOS circuit for NOR gate.	02			
		Design and implement following function using 4:1 multiplexer $F=\sum m(1,3,4,5)$	04			
Q3	а	Draw and explain TTL to CMOS interface.	04			
	b	What do you mean by multiplexure tree? Explain.	02			
		OR				

Q4 Give comparisons between TTL, ECL and CMOS logic families. 04 а

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b	What do you mean by priority encoder?	02				
а	Draw and explain SR Flip Flop using NAND gates.	02				
b	Convert D to T flipflop	04				
OR						
а	What is clock skew and clock jittering in synchronous circuits?	02				
b	Design a mod-6 synchronous counter.	04				
а	Compare Mealy machine with Moore machines.	02				
b	Design a sequence detector to detect the sequence 110, using JK flip-flops. Use Mealy Machine	04				
	b a b a b b	 b What do you mean by priority encoder? a Draw and explain SR Flip Flop using NAND gates. b Convert D to T flipflop OR a What is clock skew and clock jittering in synchronous circuits? b Design a mod-6 synchronous counter. a Compare Mealy machine with Moore machines. b Design a sequence detector to detect the sequence 110, using JK flip-flops. Use Mealy Machine 				

OR

Q8 Reduce following state diagram



06

07

- Q9aDraw and explain CPLD with it's block diagram.06
 - b Design seven-segment decoder using PLA.

OR

Q10	а	Differentiate between static and dynamic RAM?	04
	b	Compare between different types of PLDs.	03

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	С	Implement following function using PLA	
		$F_1(A, B, C) = \sum M(0, 2, 5, 7)$	
		$F_2(A, B, C) = \sum M(2, 3, 4, 5)$	06
Q11	а	Differentiate between signals and variables.	04
	b	What is a structural type of modeling? Explain with an example	04
	с	Write VHDL code for 3:8 decoder using case statement	05
		OR	
Q12	а	Explain architecture with different modeling styles.	06
	b	Explain the difference between concurrent and sequential statements.	04
	С	Explain loop statement with example.	03

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