Total No. of Questions—**8**] [Total No. of Printed Pages—**3**

Seat No.	

[4757]-1050

S.E. (Elex/E & TC) (First Semester) EXAMINATION, 2015

DIGITAL ELECTRONICS

(2012 Pattern)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Figures to the right indicate full marks.

(*ii*) Neat diagrams must be drawn wherever necessary.

(*iii*) Assume suitable data, if necessary.

1. (*a*) Draw and explain the working of two input TTL NAND gates (with totem pole). [6]

(*b*) Implement the following function using single 8 : 1 MUX. [6]

$$F(A, B, C, D) = \Sigma m\ (1, 4, 6, 8, 10, 11, 13, 14)$$

Or

2. (*a*) Design and implement full adder using suitable decoder. [6]

(*b*) Draw and explain the working of 2 i/p CMOS NOR gate. [6]

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3. (*a*) Design mod 6 ripple up counter using T flip-flops. [6]

(*b*) Convert D to T and vice versa. [6]

Or

4. (*a*) Explain moore circuit with example. Also compare moore and mealy circuit. [6]

(*b*) Design a sequence detector to detect sequence 1101 using D FF and mealy machine. [6]

5. (*a*) Compare between PROM and PAL. [5]

(*b*) A combinational circuit is defined by a function $F_1 = \Sigma m(1, 3, 5)$ $F_2 = \Sigma m\ (5, ,6, 7)$.

Implement the circuit with PLA having 3 inputs, 3 product terms and two outputs. [8]

Or

6. (*a*) Explain in detail the architecture of CPLD. [6]

(*b*) What is meant by EPROM ? State its advantages and disadvantages. [7]

7. (*a*) Explain the following statements with examples : [6]

(*i*) Process

(*ii*) Case

(*iii*) If else

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(*b*) Write a VHDL code for 8 : 1 multiplexer using behavioural modeling. [7]

Or

8. (*a*) Explain in detail signal and variable with example in VHDL. [6]

(*b*) Write a VHDL code for 4-bit ALU using case statement. [7]

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