Total No. of Questions—**8**] [Total No. of Printed Pages—**3**

Seat No.	

[5352]-135

SE (E & TC/ELECT) EXAMINATION, 2018

DIGITAL ELECTRONICS

(2012 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Neat diagrams must be drawn wherever necessary.

(*ii*) Figures to the right indicate full marks.

(*iii*) Assume suitable data, if necessary.

1. (*a*) State the following characteristics of digital TTL and CMOS ICS : [6]

(1) Noise Margins

(2) Propagation Delay Time

(3) Current Parameters.

(*b*) Explain the design of full adder using 8 : 1 Multiplexer IC. [6]

Or

2. (*a*) Draw and explain the working of two input CMOS NOR gate. [6]

(*b*) Design a 2-bit comparator circuit using gates. [6]

P.T.O.

3. (*a*) Differentiate between Moore and Mealy machine with example. [6]

(*b*) Explain the design of J-K latch using 2-input NAND gates. [6]

Or

4. (*a*) Design a sequence generator circuit to generate the following sequence 101 using non-overlapping technique. [6]

(*b*) Explain the following basic steps used to design the state machines : [6]

(1) State Diagram

(2) State Table

(3) State Reduction.

5. (*a*) With neat diagram, explain in brief the architecture of FPGA. [6]

(*b*) What is PAL ? Explain the various types of PALs ? [7]

Or

6. (*a*) Obtain a 1024 × 8 (RAM) memory using 256 × 8 memory chips. [7]

(*b*) Implement the following Boolean functions with a PLA : [6]

$$F1(A, B, C) = \Sigma M(0, 1, 2, 4)$$

$$F2(A, B, C) = \Sigma M(3, 5, 6, 7)$$

7. (*a*) Write a VHDL code for D Flip-flop using synchronous reset input. [6]

(*b*) Explain the difference between concurrent statement and sequential statement in VHDL. [4]

(*c*) Write a short note on entity. [3]

Or

8. (*a*) Write a VHDL code for 4 : 1 Multiplexer. [6]

(*b*) Write a short note on data objects in VHDL. [4]

(*c*) Explain signal and variable used in VHDL. [3]