

Total No. of Questions : 8]

SEAT No. :

P1005

[Total No. of Pages : 2

[4457]-181

S.E. (Electronics & Telecommunication) (Semester - I)

DIGITAL ELECTRONICS

(2012 Course)

Time : 2 Hours]

[Max. Marks : 50

Instructions to the candidates :

- 1) Figures to the right indicate full marks.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Assume suitable data if necessary.

- Q1)** a) Draw and explain the working of 2 input CMOS NAND gate. [6]
b) Design the following logic expression using single 8:1 multiplexer.

$$F(A,B,C,D) = \Sigma m(0,2,3,6,8,9,14) + d(12,13) \quad [6]$$

OR

- Q2)** a) With the neat diagram explain the interfacing of the CMOS as a driver and TTL as a load. [6]
b) Design a 2 bit magnitude comparator using suitable decoder. [6]
- Q3)** a) Draw and explain the diagram of JK Flip-flop using nand gates and explain how race around condition is avoided ? [6]
b) Design a sequence detector to detect the sequence 101 using Mealy machine. [6]

OR

- Q4)** a) Design a pulse train generator to generate the following sequence10110.... using shift register. [6]
b) Explain : [6]
i) Rules for state assignments.
ii) State reduction.

- Q5)** a) Design BCD to Excess-3 code converter using PAL. [8]
b) Explain the difference between PLA and PAL. [5]

P.T.O.

OR

- Q6)** a) Design the following multiple output function using PLA.
F1(a,b,c,d)= $\Sigma m(3,7,8,9,11,15)$
F2(a,b,c,d)= $\Sigma m(3,4,5,7,10,14,15)$ [7]
b) Explain the general architecture of CPLD. [6]
- Q7)** a) Explain the different modelling styles in VHDL with suitable examples. [6]
b) Write the VHDL code for a negative edge-triggered 'D' flip-flop with Synchronous active low reset input. [7]

OR

- Q8)** a) Explain the syntax of the process statement. What are the statements which can be used under the process? [6]
b) Write a VHDL code for full subtractor using structural modelling style. [7]

