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[4857]-1045

S.E. (Electronics/E and Telecommunication)

(First Semester) EXAMINATION, 2015

DIGITAL ELECTRONICS

(2012 PATTERN)

Time : Two Hours

Maximum Marks : 50

- N.B. :—** (i) Figures to the right side indicate full marks.
(ii) Neat diagram must be drawn wherever necessary.
(iii) Assume suitable data, if necessary.

1. (a) State the following characteristics of digital TTL and CMOS IC's : [6]
(i) Speed of operation
(ii) Noise margin
(iii) Figure of merit.
- (b) Implement the following function using single 4 : 1 mux : [6]
$$F(A B C D) = \sum m (2, 4, 5, 7, 10, 14)$$

Or

2. (a) Draw and explain the working of 2 input CMOS NAND gate. [6]
(b) Design and implement full adder circuit using 3 : 8 decoder. [6]
3. (a) Design and implement a synchronous up decade counter using D FF. [6]
(b) Convert D to T and T to D FF. [6]

P.T.O.

Or

4. (a) Compare Moore and Mealy circuit with suitable example. [6]
(b) Design a circuit to generate sequence 0-2-5-4-7-3 using T FF. [6]
5. (a) Compare between PROM, PAL, PLA. [5]
(b) A combinational circuit is define by a function $F_1 = \sum m (1, 3, 5)$, $F_2 = \sum m (5, 6, 7)$. Implement the circuit with a PLA having 3 inputs, 3 product terms and two outputs. [8]

Or

6. (a) Compare between CPLD and FPGA. [5]
(b) Draw a neat diagram of one cell of static and dynamic RAM with its working. [8]
7. (a) What are different types of architecture in VHDL ? Explain in detail. [7]
(b) Write a VHDL code for binary to gray code convertor. [6]

Or

8. (a) What is the difference between concurrent and sequential statement in VHDL. Explain with proper example. [7]
(b) Write a VHDL code for D FF using synchronous reset input. [6]