Total No. of Questions—8]　　　　[Total No. of Printed Pages—3

Seat
No.

[5057]-250

S.E. (E&TC)/Electronics (First Semester) EXAMINATION, 2016

DIGITAL ELECTRONICS

(2012 PATTERN)

Time : Two Hours　　　　　　　　　　Maximum Marks : 50

N.B. :— (i) Attempt Q. **1** or Q. **2**, Q. **3** or Q. **4**, Q. **5** or Q. **6** and Q. **7** or Q. **8**.

(ii) Neat diagrams must be drawn wherever necessary.

(iii) Figures to the right indicate full marks.

(iv) Assume suitable data, if necessary.

(v) Use of logarithmic tables, slide rule and electronic non-programmable calculator is allowed.

1. (a) Compare TTL, CMOS and ECL. [6]

(b) Obtain an 8 : 1 multiplexer with a dual 4-line to 1-line multiplexers having separate enable inputs but common selection lines. [3]

(c) Explain the working of CMOS Inverter. [3]

Or

2. (a) Design 2-bit comparator using decoder. [6]

(b) What do you mean by tristate logic ? Explain in detail one application of such logic circuit. [3]

(c) Explain the concept of look ahead carry generator and advantage of the same. [3]

P.T.O.

3. (*a*) Explain the following terms : [6]

      (*i*)   State Table

      (*ii*)   State Diagram

      (*iii*) State Reduction.

    (*b*) Design 4-Bit Excess-3 to BCD Code Converter and implement using Logic Gates. [6]

Or

4. (*a*) Write a short note on ALU. [5]

    (*b*) By using suitable FF'S design A counter to go through states 0-1-3-4-6-0. Draw the logic diagram. Examine the action of counter for the Unused States. [7]

5. (*a*) Give comparison between PROM, PLA and PAL. [5]

    (*b*) A combination circuit is defined by the function : [8]

F1(A, B, C) = Σm(2, 3, 7)

F2(A, B, C) = Σm(3, 4, 6)

Implement the Circuit using PLA.

Or

6. (*a*) Compare between CPLD and FPGA. [6]

    (*b*) Design a BCD to gray code converter and implement using PLA. [7]

7. (a) Write a VHDL code for 4-Bit Binary to gray code converter using CASE statement. [8]

(b) What is the difference between Concurrent and Sequential statement in VHDL ? Explain with proper example. [5]

Or

8. (a) Write a VHDL code for a 2-Bit Comparator using Data flow Modelling Technique. [7]

(b) Explain different classes of data Objects in VHDL with example for each. [6]