

Total No. of Questions—8]

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| Seat No. | |
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[5252]-135

S.E. (Electronics & Telecommunication) (Semester-I)

EXAMINATION, 2017

DEGITAL ELECTRONICS

(2012 PATTERN)

Time : Two Hours

Maximum Marks : 50

N.B. :— (i) Figures to the right indicate full marks.

(ii) Neat diagrams must be drawn wherever necessary.

(iii) Assume suitable data, if necessary.

1. (a) Define and explain : [8]
- (i) Fan out
 - (ii) Noise Margin
 - (iii) Propagation Delay
 - (iv) Power Dissipation
- (b) Write a short note on look ahead carry generator. [4]

Or

2. (a) Explain with neat diagram interfacing of TTL gate driving CMOS gate and vice versa. [6]
- (b) Design an even parity generator circuit for 4-bit input using multiplexer. [6]

P.T.O.

3. (a) Explain the difference between combinational and sequential circuits. [4]
- (b) Design a sequence detector to detect the following sequence using D flip-flop -- 110 -- [8]

Or

4. (a) Explain : [6]
- (i) State Table
- (ii) State Diagram
- (iii) State Assignment.
- (b) Convert JK FF to T FF. [6]

5. (a) Explain the difference between CPLD and FPGA. [6]
- (b) Implement the following functions using PLA : [7]
- $$F_1(A, B, C) = \Sigma m(2, 3, 7)$$
- $$F_2(A, B, C) = \Sigma m(3, 4, 6)$$

Or

6. (a) Design a BCD to excess 3 code converter and implement it using PAL [8]
- (b) Explain difference between PLA and PAL. [5]
7. (a) Explain the difference between concurrent statement and sequential statement in VHDL. [6]
- (b) Write the VHDL code for 4-bit ripple up-counter. [7]

Or

- 8.** (a) Explain the following statements used in VHDL with suitable examples : [8]
- (i) Entity
 - (ii) Architecture
 - (iii) Process
 - (iv) IF
- (b) Write the VHDL code for D flip-flop using asynchronous reset input. [5]