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# S.E. 2012 (E\&TC Engineering) <br> Integrated Circuits (204187) (Semester-II) 

## Time: 2 Hours

Max. Marks : 50
Instructions to the candidates:

1) Neat diagrams and waveforms must be drawn wherever necessary.
2) Figures to the right side indicate full marks.
3) Use of Calculator is allowed.
4) Assume Suitable data if necessary.

Q1) a) State any four characteristics of an ideal OPAMP?
b) A dual input, balanced-output (DIBO) differential amplifier has following specifications: $\mathrm{R}_{\mathrm{C} 1}=\mathrm{R}_{\mathrm{C} 2}=2.2 \mathrm{~K} \Omega, \mathrm{R}_{\mathrm{E}}=4.7 \mathrm{~K} \Omega, \mathrm{R}_{\text {in } 1}=\mathrm{R}_{\text {in } 2}=50 \Omega,+\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$, $-\mathrm{V}_{\mathrm{EE}}=-10 \mathrm{~V}, \beta_{\mathrm{dc}}=\beta_{\mathrm{ac}}=100$ and $\mathrm{V}_{\mathrm{BE}}=0.715 \mathrm{~V}$. Calculate
i) ICQ
ii) $\quad V_{\text {CEQ }}$
iii) Voltage gain: $A_{d}$
c) Why frequency compensation is required in OPAMP? Explain dominant pole compensation with circuit \& frequency response.

OR
Q2)
a) Give the classification of ICs according to number of components per chip?
b) An inverting amplifier using IC741 OPAMP has flat frequency response up to 40

KHz , voltage gain of 10 . Find maximum peak - to peak input voltage to get maximum distortion less output?
c) Why level shifter / translator is needed in an OPAMP? What are its different types?

Explain level shifter with constant current bias using diodes.

Q3) a) Draw an inverting summing amplifier with three inputs? Derive an expression for its output voltage $\mathrm{Vo}=-(\mathrm{Va}+\mathrm{Vb}+\mathrm{Vc})$.
b) Draw half wave precision rectifier \& explain its operation in brief?
c) Draw an inverting comparator using OPAMP with +ve reference \& explain its operation in brief with waveforms?

## OR

a) For an inverting Schmitt trigger $\mathrm{R} 1=100 \Omega, \mathrm{R} 2=56 \mathrm{~K} \Omega$ (where R 2 is connected in feedback path). If Vin $=1 \mathrm{~V}_{(\mathrm{P}-\mathrm{P})}$ sine wave and $\mathrm{Vs}= \pm 15 \mathrm{~V}$, calculate:
i) $V_{U T} \& V_{L T}$
b) Draw \& explain in brief an instrumentation amplifier interfaced with RTD bridge for temperature measurement.
c) Draw \& explain in brief a sample \&hold circuit with waveforms?

Q7) a) Draw the block schematic of PLL and explain each block in detail.

Q5)

Q6)

Q8)
a) In a V-I converter with grounded load, $\mathrm{Vin}=5 \mathrm{~V}, \mathrm{R}=10 \mathrm{~K} \Omega$ and voltage at noninverting terminal is 1 V . Assuming that OPAMP is initially nulled, Calculate:
i) Load current
ii) The output voltage Vo
b) Draw a 2-bit D/A converter with R-2R resistors \& explain its operation? State its advantages?
c) Explain various specifications of A/D converter.

OR
a) Draw an I-V converter and derive an expression for its output voltage (Vo)?
b) Draw \& explain 2-bit flash type analog to digital converter (ADC)
c) An 8-bit D / A converter has a resolution of $10 \mathrm{mV} /$ bit. Find the analog output voltage for the following digital inputs:
i) 10001010
ii) 00010000
b) Design an adjustable voltage regulator using LM317 for following specifications:

Output voltage, $\mathrm{Vo}=5 \mathrm{~V}$ to 12 V
Output current, $\mathrm{Io}=1 \mathrm{~A}$ and $\mathrm{R} 1=240 \Omega(\mathrm{R} 1$ is connected between $\mathrm{o} / \mathrm{p}$ terminal \& adj terminal).
c) Explain the following terms:
i) Load regulation
ii) Line regulation

## OR

a) For a PLL 565, the free running frequency is $2.5 \mathrm{KHz},+\mathrm{Vcc}=+10 \mathrm{~V},-\mathrm{V}_{\mathrm{EE}}=-10 \mathrm{~V}$.

If demodulation capacitor ( C 2 ) is $10 \mu \mathrm{~F}$, find lock range \& capture range.
b) State applications of PLL? Also draw block diagram of FSK demodulator.
c) Draw \& explain a three terminal voltage regulator with current boosting.

