Total No. of Questions : 8]

SEAT No. :

P3595

[Total No. of Pages : 2

[5152]-136
S.E.(Electronics/Electronics & Telecommunication)
INTEGRATED CIRCUITS (Semester -II)
(2012 Pattern)

Time : 2 Hours] *[Maximum Marks : 50*

Instructions to the candidates:

1) *Answer Q1 or Q2, Q3 or Q4, Q5, or Q6 and Q7 or Q8.*

2) *Neat diagrams must be drawn wherever necessary.*

3) *Figures to the right indicate full marks.*

4) *Use of electronic pocket calculator is allowed.*

5) *Assume suitable data, if necessary.*

Q1) a) Derive the expression for I_{CQ} and V_{CEQ} for dual input balanced output difference amplifier using r-parameters. **[6]**

b) Define and explain following terms with respect to Op-Amp: slew Rate, input Bias Current & input offset voltage. **[6]**

OR

Q2) a) What is the need of frequency compensation? Explain dominant pole method of external frequency compensation. **[6]**

b) With neat diagram explain block diagram of Op-Amp and function of each block. **[6]**

Q3) a) What are the problems associated with the ideal differentiator? Draw neat circuit diagram of practical differentiator and explain its operation with its frequency response. **[6]**

b) Draw and explain Non inverting amplifier using Op-amp. Derive the expression for its output voltage. **[6]**

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OR

Q4) a) Explain the necessity of Precision rectifier and explain the operation of half wave precision rectifier with neat circuit diagram. **[6]**

b) Draw and explain operation of inverting Schmitt trigger using Op-amp with neat waveforms. **[6]**

Q5) a) With the help of neat diagram explain the operation of Weighted binary resistor type of DAC. **[7]**

b) Draw neat diagram and V to I convertor with floating load and explain its operation. **[6]**

OR

Q6) a) Calculate output voltage of 8 bit DAC for digital input 10000000, 11111111 & 11110000 with reference voltage of 5V. **[6]**

b) With the help of neat diagram explain the operation of Flash type ADC. **[7]**

Q7) a) Draw and explain circuit of Frequency synthesizer using PLL. **[7]**

b) Draw neat diagram and explain three terminal adjustable voltage regulator with expression for output voltage. **[6]**

OR

Q8) a) Explain operation of PLL with the help of neat block diagram. Define the terms Lock range and capture range. **[7]**

b) Explain three terminal positive voltage regulator with typical circuit diagram. What are various output voltages available from such different ICs? **[6]**

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