Total No. of Questions—**8**] [Total No. of Printed Pages—**3**

Seat No.	

[5352]-136

S.E. (E&TC/Elect.) (II Sem.) EXAMINATION, 2018
INTEGRATED CIRCUITS
(2012 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. :— (*i*) Answer Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6**, Q. No. **7** *or* Q. No. **8**.
(*ii*) Neat diagrams must be drawn wherever necessary.
(*iii*) Figures to the right indicate full marks.
(*iv*) Use of electronic pocket calculator is allowed.
(*v*) Assume suitable data, if necessary.

Q. 1 **(a)** Draw the block diagram of op-amp and explain the function of each block in detail. **[04]**

(b) Define the following op-amp parameters. **[04]**

1) Slew rate
2) CMRR
3) Input offset voltage
4) PSRR

(c) State and compare different op-amp technologies. **[04]**

OR

Q. 2 **(a)** What is the need of frequency compensation? Explain any one method of external frequency compensation. **[06]**

(b) The dual input balanced output difference amplifier has following specifications. **[06]**

R_C =2.5kΩ, R_E=4.8kΩ, $R_{b1}=R_{b2}=R_b$=50Ω, $+V_{CC}$ = +10V, $-V_{EE}$ = -10V, β =100, V_{BE} = 0.8V. Assume h_{ie} = 1.1kΩ. Calculate:

1) Q-point values
2) Voltage gain
3) Input & Output Resistance

P.T.O.

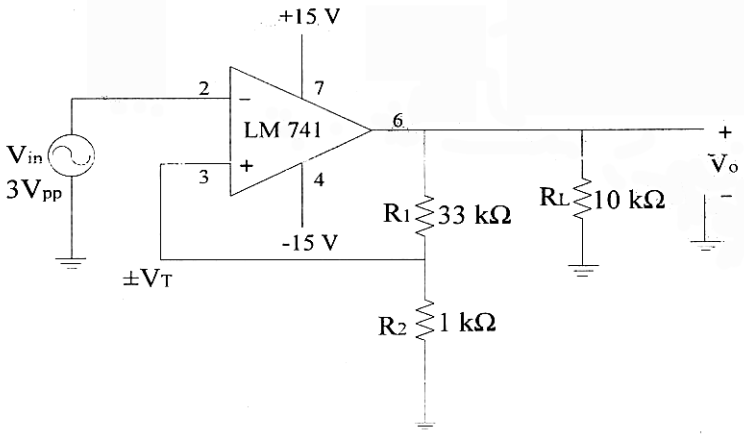
Q. 3 **(a)** Why ideal integrator is required to be modified? Draw the practical integrator and explain its operation with frequency response. **[06]**

(b) Draw and explain precision half wave rectifier circuit using op-amp. **[04]**

(c) List out the characteristics of a typical/good instrumentation amplifier. **[02]**

OR

Q. 4 **(a)** For the Inverting Schmitt trigger shown below, Calculate UTP, LTP & hysteresis width. Draw input & output waveforms. Also comment on Hysteresis loop. **[06]**



(b) Draw a neat circuit diagram of two inputs inverting summing amplifier using op-amp & obtain expression for output voltage. **[06]**

Q. 5 **(a)** Draw the circuit diagram and explain working of voltage mode R-2R ladder DAC. **[05]**

(b) Explain grounded load V to I converter with necessary derivation. **[04]**

(C) Explain current to voltage converter using Op-amp. **[04]**

OR

Q. 6 **(a)** Write a note on 2 bit Flash type analog to digital converter (ADC). **[06]**

(b) A 5 bit R-2R ladder network with reference voltage of 10V. Find **[07]**

1) Analog output due to LSB change.
2) Full scale output voltage
3) Analog output for digital input 11001

Q. 7 **(a)** Explain the operation of PLL using a neat block diagram. Define the terms Centre frequency and capture time related to PLL. **[06]**

(b) Explain low drop-out regulator. **[04]**

(c) Explain frequency multiplier using PLL. **[03]**

OR

Q. 8 **(a)** Calculate output frequency f_o, lock range and capture range of PLL if the timing parameters are C_T=0.1μf, R_T=1kΩ. The filter capacitor is 10μf. **[06]**

(b) Draw a neat diagram and explain three terminal adjustable voltage regulator with expression for output voltage. **[07]**