Total No. of Questions—**8**] [Total No. of Printed Pages—**3**

Seat No.	

[4857]-1046

S.E. (Electronics/E&TC Engineering)

(Second Semester) EXAMINATION, 2015

INTEGRATED CIRCUITS

(2012 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Neat diagrams and waveforms must be drawn wherever necessary.

(*ii*) Figures to the right side indicate full marks.

(*iii*) Use of calculator is allowed.

(*iv*) Assume suitable data if necessary.

1. (*a*) The following specifications are given for the DIBO differential amplifier : [6]

R_E = 4.7 kΩ, R_C = 2.2 kΩ, R_{in1} = R_{in2} = 50 Ω, V_s = ± 10 V and the transistor with β_{ac} = β_{dc} = 100 with V_{BE} = 0.7 V.

(*i*) Determine the I_{CQ} and V_{CEQ} values.

(*ii*) Determine the voltage gain.

(*b*) With neat circuit, explain the dominant pole frequency compensation technique. [6]

Or

2. (*a*) Design a DIBO differential amplifier with a constant current bias using diodes to satisfy the following requirements :[6]

Differential voltage gain Ad = ±10

Current supplied by the constant current bias circuit = 4 mA

Supply voltage V_S = ± 12 V

(*b*) Write a note on noise in op-amp. [6]

P.T.O.

3. (*a*) Explain virtual ground concept and virtual short concept. [6]

(*b*) With neat circuit diagram and waveforms, explain working of half wave precision rectifier. [6]

Or

4. (*a*) Explain sample and hold circuit using op-amp. [6]

(*b*) What are the limitations of ideal integrator ? How are they overcome in practical integrators ? [6]

5. (*a*) With neat circuit diagram, explain current to voltage converter. [5]

(*b*) Draw the neat circuit diagram of R–2R ladder digital to analog converter (DAC) and explain its working. [5]

(*c*) What output voltage would be produced by a D/A converter whose output range is 0 to 10 V and input binary number is : [3]

(*i*) 10 (for a 2-bit DAC converter)

(*ii*) 0110 (for a 4-bit DAC)

(*iii*) 10111100 (for a 8-bit DAC).

Or

6. (*a*) Explain the operation of successive approximation type analog to digital converter. [5]

(*b*) With neat circuit diagram, explain V to I converter with grounded load. [5]

(*c*) List various specifications of ADC. [3]

7. (*a*) Explain the following : [10]

(*i*) Digital phase comparator used in PLL

(*ii*) PLL as a FSK demodulator.

(*b*) For LM317 adjustable voltage regulator, R_1 = 240 Ω and R_2 = 2 kΩ. If I_{adj} = 50 μA and V_{ref} = 1.25 V. Find value of V_o. [3]

Or

8. (*a*) Define the following terms with reference to PLL : [10]

(*i*) Free running frequency

(*ii*) Lock range

(*iii*) Capture range

(*iv*) Pull-in-time.

(*b*) Explain low drop-out regulator. [3]