Seat	
No.	

[5057]-246

S.E. (Electronics/Electronics & Telecommunication)

(Second Semester) EXAMINATION, 2016

INTEGRATED CIRCUITS

(2012 **PATTERN**)

Time: Two Hours

Maximum Marks: 50

- N.B. :— (i) Answer Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4, Q. No. 5 or Q. No. 6, Q. No. 7 or Q. No. 8.
 - (ii) Neat diagrams must be drawn wherever necessary.
 - (iii) Figures to the right indicate full marks.
 - (iv) Use of electronic pocket calculator is allowed.
 - (v) Assume suitable data, if necessary.
- 1. (a) What is the need of frequency compensation? Explain dominant pole method of external frequency compensation. [6]
 - (b) With neat diagram explain the necessity and working of current mirror circuit. [6]

P.T.O.

2.	(a)	The following	lowing	spe	cifications	are	given	for	dual	input	balance
		output	differen	nce	amplifier	:					

Determine:

- (i) Operating point i.e. I_{CQ} and V_{CEQ}
- (ii) Input and output resistance. [6]
- (b) What are the different types of noise those are associated with op-amps? Draw op-amp noise model and give expression for output noise voltage. [6]
- 3. (a) Explain practical integrator circuit with neat circuit diagram.

 What are the limitations of ideal integrator? [6]
 - (b) Draw and explain sample and hold circuit using Op-amp. [6] Or
- **4.** (a) Draw and explain half wave precision rectifier circuit. [6]
 - (b) Explain the working of inverting Schmitt trigger. Also derive the equations for the trigger points. [6]
- **5.** (a) Explain F2V converter with appropriate waveforms. [7]
 - (b) Explain binary weighted resistor type of DAC. [6]

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6.	(a)	With the help of neat diagram explain the operation of flash
		type ADC. [7]
	(<i>b</i>)	Calculate output voltage of 8 bit DAC for digital input 10000000
		and 11011101 with reference voltage of 10 V. [6]
7.	(a)	Explain operation of PLL with the help of neat block diagram.
		Define the terms lock range and capture range. [7]
	(<i>b</i>)	Write a short note on fixed and variable voltage regulators. [6]
		Or
8.	(a)	Draw and explain circuit of FM demodulator using PLL.[7]
	(<i>b</i>)	Explain low drop out voltage regulator. [6]