Total No. of Questions—**8**] [Total No. of Printed Pages—**2**

Seat No.	

[5352]-163

S.E. (Computer Engineering) (I Sem.) EXAMINATION, 2018
DIGITAL ELECTRONICS AND LOGIC DESIGN
(2012 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. :— (*i*) Answer Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6**, Q. No. **7** *or* Q. No. **8**.
(*ii*) Figures to the right indicate full marks.
(*iii*) Assume suitable data, if necessary.

Q1) a) Minimize the following function using K-map & realize using Logic gates. [4]
$F(A,B,C,D) = \sum m(1,5,7,13,15)\ d(0,6,12,14)$

b) Convert following : [2]
$(46)_{10} = (?)_8$

c) List the differences between CMOS and TTL [6]

OR

Q2) a) Convert the following numbers into binary numbers. [4]
i) $(37)_8$ ii) $(25.5)_{10}$

b) Explain standard TTL Characteristics in detail [6]

c) Represent the following signed number in 2s complement method: [2]
i) + 25 ii) -25

Q3) a) Design a 3-bit Excess 3 to 3-bit BCD code converter using logic gate. [6]

b) Design Mod-5 synchronous counter using JK FFs. [4]

c) Draw the excitation table of J-K Flip-flop. [2]

P.T.O.

OR

Q4) a) Design a 4-bit Binary to Gray code converter circuit using logic gates [4]

b) Design a Mod 20 counter using decade counter IC 7490 [6]

c) Perform the following: [2]

$$(11011)_2 + (0101)_2 = (?)_2$$

Q5) a) State and explain basic component of ASM chart? Also explain the Salient features of ASM chart? [7]

b) Write VHDL code 4:1 Multiplexer using Behavioral and Dataflow modeling style. [6]

OR

Q6) a) Design a sequence generator circuit to generate the sequence 1-2-3-7-1 using Multiplexer Controller based ASM approach. [7]

Consideration :

i) If control input C = 0, the sequence generator circuit in the same state.

ii) If control input C = 1, the sequence generator circuit goes into next state.

b) Explain the following statements used in VHDL with suitable examples: [6]

i) CASE.

ii) With - Select - When.

iii)Loop statement.

Q7) a) Comparison between PROM, PLA and PAL [7]

b) Draw and explain the basic architecture of FPGA. [6]

OR

Q8) a) A combinational circuits is defined by the function [7]

$F_1(A,B,C) = \sum m(0,1,3,7)$

$F_2(A,B,C) = \sum m(1,2,5,6)$

Implement this circuit with PLA.

b) A combinational circuits is defined by the function [6]

$F_1(A,B,C) = \sum m(0,1,5,6,7)$

Implement this circuit with PAL.