Total No. of Questions : 8]

SEAT No. :

P1020

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## S.E. (Computer Engineering) (Semester - I)

## DIGITAL ELECTRONICS AND LOGIC DESIGN

## (2012 Course)

*Time :2 Hours]* *[Max. Marks :50*

***Instructions to the candidates :***

1) ***Attempt Q.No.1 or Q.No.2, Q.No.3 or Q.No.4, Q.No.5 or Q.No.6 and Q.No.7 or Q.No.8.***
2) ***Figures to the right indicate full marks.***
3) ***Assume suitable data, if necessary.***

***Q1)*** a) Minimize the following function using K-map & realize using Logic gates.

$F(A,B,C,D) = \sum m(1,3,7,11,15) + d(0,2,5)$ . **[4]**

b) Convert following : **[2]**

$(255)_{10} = (?)_{16}$

c) Differentiate between standard TTL and CMOS logic circuit w.r.t. **[6]**

i) Propagation delay ii) FANOUT

iii) Figure of merit

OR

***Q2)*** a) Convert the following numbers into binary and hexadecimal numbers. **[4]**

i) $(46)_8$ ii) $(20.5)_{10}$

b) Define the following terms and mention its standard values for TTL family. **[6]**

i) Voltage and Current parameter.

ii) Power Dissipation.

iii) Noise margin.

c) Represent the following signed number in 2's complement method : **[2]**

i) +8 ii) -8

***Q3)*** a) Design a 4-bit BCD to Excess-3 code converter circuit using minimum number of logic gates. **[6]**

b) Design Mod-5 synchronous counter using JK FFs. **[4]**

c) Draw the excitation table of S-R Flip-flop. **[2]**

***P.T.O.***

OR

***Q4)*** a) Design a 3-bit binary to 3-bit gray code converter using IC-74138. **[4]**

b) How many Flip-flops are required to build a binary counter circuit to count from 0 to 2048. What is the frequency of the output of last Flip-flop for an input clock frequency of 6MHz? **[6]**

c) Perform the following : **[2]**

$(1111)_2 + (1111)_2 = ?$

***Q5)*** a) State and explain basic component of ASM chart? What is difference between ASM chart and conventional flow chart? **[7]**

b) Write VHDL code 8:1 Multiplexer using Behavioral and Dataflow modeling style. **[6]**

OR

***Q6)*** a) Design a sequence generator circuit to generate the sequence 1-3-5-7 using Multiplexer Controller based ASM approach. **[7]**

Consideration :

i) If control input C = 0, the sequence generator circuit in the same state.

ii) If control input C = 1, the sequence generator circuit goes into next state.

b) Explain the following statements used in VHDL with suitable examples: **[6]**

i) Process.

ii) CASE.

iii) With-Select-When.

***Q7)*** a) What are different types of PLDs? Design 3:8 decoder using PLD. **[7]**

b) Draw and explain the basic architecture of FPGA. **[6]**

OR

***Q8)*** a) A combinational circuits is defined by the function **[7]**

$F_1(A,B,C) = \sum m(0,1,2,4)$

$F_2(A,B,C) = \sum m(1,3,5,6)$

Implement this circuit with PLA.

b) A combinational circuits is defined by the function **[6]**

$F_1(A,B,C) = \sum m(0,1,3,4)$

Implement this circuit with PAL.