Total No. of Questions—**8**] [Total No. of Printed Pages—**3**

Seat No.	

[5057]-253

S.E. (Computer Engineering) (First Semester)

EXAMINATION, 2016

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2012 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Attempt Q. No. **1** *or* Q. No. **2,** Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6,** Q. No. **7** *or* Q. No. **8**.

(*ii*) Figures to the right indicate full marks.

(*iii*) Assume suitable data, if necessary.

1. (*a*) Do the required conversions for the following numbers : [6]

(*i*) $(205.76)_{10} = (\ )_2$

(*ii*) $(7A2B)_{16} = (\ )_8$

(*iii*) $(6516)_{10} = (\ )_{16}$

(*b*) Define the following terms for TTL family : [2]

(*i*) Fan Out

(*ii*) Speed of Operation.

(*c*) Explain the operation of CMOS NOR gate. [4]

Or

2. (*a*) Minimize the following functions using K-map and realize using logic gates : [4]

$F(A, B, C, D) = \Sigma m(0, 2, 8, 10, 14)$.

P.T.O.

(*b*) Perform the following operation using 2's complement method : [2]

$$(27)_{10} - (14)_{10} = (?).$$

(*c*) Explain the working of three input TTL NAND gate with Totem-pole output. [6]

3. (*a*) Implement the following function using 4 : 1 multiplexer : [4]

$F(A, B, C, D) = \Sigma m(0, 3, 7, 9, 11, 14, 15)$.

(*b*) Convert the following Gray code numbers to Binary : [2]

(*i*) $(101101)_2$

(*ii*) $(111111)_2$

(*c*) What are the applications of Flip-Flops ? Explain the working of SR Flip-Flop. [6]

Or

4. (*a*) Explain with suitable equations and diagrams concept of look ahead carry Generator for 4-bit adder circuit. [6]

(*b*) Design MOD 76 counter by using IC 7490. [6]

5. (*a*) Explain the following modelling styles of VHDL with suitable example : [6]

(*i*) Behaviour modelling style

(*ii*) Data flow modelling style.

(*b*) What is ASM chart ? Explain components of ASM chart. What are applications of ASM chart in digital system design ? [7]

Or

6. (*a*) Draw an ASM chart and state table for 3-bit Up counter having control input E : [7]

(*i*) If control input E = 0 : Counter remains in same state

(*ii*) If control input E = 1 : Counter goes to next state.

(*b*) What is VHDL ? Explain entity and architecture declaration in VHDL with suitable example. [6]

7. (*a*) Draw and explain the basic architecture of FPGA. [6]

(*b*) A combinational circuits is defined by the functions : [7]

$$F_1(A, B, C) = \Sigma m(0, 2, 5, 7)$$

$$F_2(A, B, C) = \Sigma m(0, 1, 6, 7)$$

Implement this circuit with PLA.

Or

8. (*a*) Comparison between PROM, PLA and PAL. [7]

(*b*) What is CPLD ? Give the difference between CPLD and FPGA. [6]